# Vivado New Project Tutorial

This tutorial guides you through the typical steps of design, simulation, synthesis and implementation of a simple project, designed from scratch, like those that you will do at the Applications for the Digital Integrated Circuits course.

## Contents

Project File Management	2
Create a New Project	3
Create Source Files	11
Add Source Files	17
Source File Editor	19
Simulation	20
I/O Ports Assignment	22
Synthesis and Implementation	22
Device Programming	26
Quick Project Guide	29

# Project File Management

The FPGA design flow goes through the stages shown in Figure 1. The Vivado IDE (Integrated Design Environment) arranges these stages in the *Flow Navigator* and guides you through it.



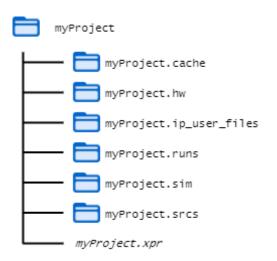


Various files are employed in each design flow stage, all of them created and managed by Vivado, except for the source files, that are written by you, the designer. All files created by Vivado reside in the project folder (directory) and its subfolders. Your source files should also reside inside the project folder.

To keep things as simple as possible, strictly follow these two rules:

- Each project has its own folder.
- All (Verilog) source files are saved in their default locations.

The project folder has the structure shown in Figure 2.





Some folders are created by Vivado at the project creation, others are created during later stages of the FPGA design flow. Most of the files are taken care of by Vivado, so you need not bother about their names or where they are located. The only files you should care about are:

- design source files
- simulation source files
- constraints file

Remember:

• All project source files should reside inside the project folder.

## Create a New Project

Open the Vivado program. Wait a couple seconds until Vivado opens the Start Page.

From the Start Page open the New Project wizard by clicking on **Create Project** option in the **Quick Start** panel (Figure 3). Alternatively you may open the New Project wizard from Vivado's main menu, selecting **File** -> **New Project ...** .



Figure 3: Quick Start panel from Vivado Start Page

The New Project wizard opens a dialog with a brief description of the wizard (Figure 4). Click **Next** to advance through the New Project wizard steps.

	New Project 🧕 🧕
VIVADO	Create a New Vivado Project This within will guide you through the creation of a new project. To create a vivado project you will need to provide a name and a location for your project files. Next, you will specify the type of flow you'll be working with. Finally, you will specify your project sources and choose a defoult part.
E XILINX.	Tente - Frain Cancel

Figure 4: New Project wizard open dialog

In step 1 (Project Name) of the New Project wizard (Figure 5) set the name of the project in the *Project Name* text editor field. The default name is project\_1, but you should change it to a more descriptive name. Vivado uses this name as a prefix for the names of the project's subfolders.

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Check the checkbox *Create project subdirectory*. You may keep the default *Project Location* (/home/student on Linux) or change it to a convenient location but be sure to create a project subdirectory such that all project files are kept in its subdirectory and not mixed with other files, unrelated to this project. If a warning message appears, telling you that a subdirectory with this name already exists, you should change the *Project Name*.

	New Project		
Project Name Enter a name for your project and specify a directory where the project	data files will be stored.		4
Project name project_1			•
Project (acation: /home/student			0
Create project subdirectory			
Project will be created at .nonwistudent/project_1			
۲	= Back	light >	Gram

Figure 5: New Project wizard step 1 (Project Name)

Click Next to continue.

In step 2 (Project Type) keep the default selection *RTL Project* (Figure 6). Click **Next** to continue.

	New Project 👋
	ect Type dy the type of project to create.
*	BTL Project You will be able to add sources, create block designs in IP integrator, generate IP, run RTL analysis, synthesis, implementation, design planning and analysis. Descriptions are extensible gkts platform Post-synthesis Project You will be able to add sources, view device resources, run design analysis, planning and implementation.
0	Dig not specify sources of the time     JO Planning Project     De not specify design sources. You will be able to view part/package resources.     Igported Project     Create a Visedo project from a Symplify, XST or ISE Project File.
0	Egample Project Create a new Vivado project from a predefined template.
(?)	< Back Back (Int > Cancel

Figure 6: New Project wizard step 2 (Project Type)

In step 3 (Add Sources) you may add design source files or create new ones (Figure 7). You may add or create files anytime later (see section Create Source Files). Click **Next** to continue.

dd it to your project. You can also ad +,     1   4	d and create sources later.	1
	Use Add Files. Add Directories or Create File buttoms being	
	Use Add Files, Add Directories or Create File buttom below	
	Add Files Add Directories Create File Suttons below	

Figure 7: New Project wizard step 3 (Add Sources)

In step 4 (Add Constraints) you may add or create constraint files (Figure 8). You may add or create them anytime later. Click **Next** to continue.

New Project	8
Add Constraints (optional) Specify or create constraint files for physical and timing constraints.	A
+,   -   +   +	
Use Add Files or Create File buttons below	
<u>àdd Files</u> <u>Create File</u> Copy constraints files into project	
? seak	Einish Cancel

Figure 8: New Project wizard step 3 (Add Constraints)

In step 5 (Default Part) of the New Project wizard (Figure 9) change the tab from Parts to Boards.

etault Part		(1944) T							
oose a default Xiirx part or	board for your proj	ect.							
Parts   Boards									
Report All Fitters									
Category: All			Package	AI I	*	Temp	anature:	All	~
Family: All			Speed	All		142012	powen	All	
			- Anna	- 17 <u>1</u>	~		Ponel.	1974 - C	
Search: Qr		w.							
Part st:7vs415tffv1157-1	VO Pin Count 1157	Available KOBs 600	LUT Elements 257600	FlipFlops 515200	Block RAME 880	Ultra RAMs	D5Ps 2160	Gb Transcer 20	vers
#C7w415tffv1158-3	1150	350	257600	515200	880	0	2160	40	-1
ac7w415tfv1158-2	1150	350	257600	515200	BBD	0	2160	48	
xc7vx415tffv1158-2L	1158	350	257600	515200	880	0	23.60	46	- 1
x:7xx415tffv1158-1	1158	350	257600	515200	880	0	2160	48	-1
xc7w415tffv1927-3	1927	600	257600	515200	880	0	2160	48	- 6
xc7vx415tffv1927-2	1927	600	257688	515200	880	0	2160	48	
#E7w415tffv1927-2L	1927	600	257600	515200	880	0	2160	48	
xc7vx415tffv1927-1	1927	600	257600	515200	880	0	2160	48	
xc?vx485tffg1157-3	1157	600	303600	607200	1030	0	2800	20	
xt;7ve485tffg1157-2	1157	600	303600	607200	1030	0	2900	20	
#:7xx485tffg1157-2L	1157	600	303600	607200	1030	0	2800	20	
wc?wv4850fg1157-1	1157	600	202600	607200	1030	0	2800	20	
xc7w485tffg1158-3	115#	350	303600	607200	1030	0	2800	48	
< :	-								-20

Figure 9: New Project wizard step 5 (Default Part)

Select the pynq-z2 board from the list of boards (Figure 10).

Parts	Boards					
Ruset A	All Filters					install/Update Boards
Vendon	Al ~	Name: AD			1.000	Board Rev. Latest
Search	0	~				
	y Name		Preview	Vendor	File Version	Part
Alpha	Oata ADM-PCE-7V3			alpha-data.com	1.1	xc7vx660t#g1157-2
Kintex	Utrascale Aphadata board		1	alpha-data.com	1.0	xcku060#wal156-2+e
	and Zyng Evaluation and Dev Imparian Card Connections		100	em.avnet.com	1.4	xc72020cig404-1
pynę-2	2			tul.com.tw	1.0	xc72020c1g400-1
	AC701 Evaluation Platform	,	No. of Street,	willins.com	1.4	xc7a200tfbg576-2

Figure 10: New Project wizard step 5 (Default Part) with the Pynq-Z2 board selected

After you selected the board click **Next**.

The last dialog of the New Project wizard (Figure 11) shows a brief description of the settings and selections you have made. Click **Finish**.

	New Project 🛛 🕘
VIVADO	New Project Summary         A new RTL project named ladder will be created.         No source files or directories will be added. Use Add Sources to add them later.         No constraints files will be added. Use Add Sources to add them later.         The default part and product family for the new project: Default Board: print add Doddigation.         Product 2ynq-7000 Product 2ynq-7000 Package: dg400 Spaed Grade: -1
E XILINX.	To create the project, click Farish           K Back         just =         Environ         Cancel

Figure 11: New Project wizard summary

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After Vivado has created and initialized the project, it opens the Project Manager window (Figure 12).

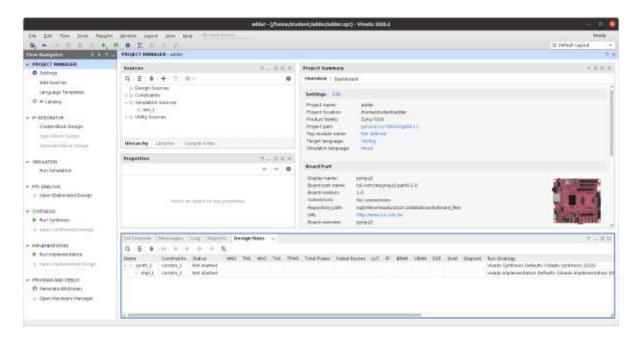


Figure 12: Vivado project manager window

## Create Source Files

To create a new design source file, click on the 'Plus' button in the *Sources* panel (Figure 13) from the project manager window.



Figure 13: Open a new source file

In the *Add Sources* dialog window that opens (Figure 14), select the file type you want to create (design source, simulation source or constraints) and click **Next**.

	Add Sources	
VIVADO	Add Sources This guides you through the process of adding and creating sources for your project Add or greate constraints # Add or create design sources Add or create gimulation sources	
E XILINX.	- Burg - Dave - Elange -	Cancel

Figure 14: Source file type selection

Alternatively, in the *Sources* panel you may right click on the desired type you want to create (Design Sources, Constraints or Simulation Sources) and from the pop-up menu select the **Add Sources** ... option (Figure 15).

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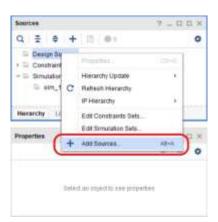


Figure 15: Open a new source file of the desired type

This alternative way opens the *Add Sources* dialog with the desired file type selected by default. Click **Next**. The next *Add Sources* dialog opens (Figure 16). You may add files to the project or create new ones. Click on **Create File** button.

+, - 1	E.			
	Une Add (	lies, Add Directories or Create	File Buttom below	

Figure 16: Add Sources window

In the small dialog box that opens (Figure 17) enter the desired name for the source file in the *File Name* text editor field, but keep unchanged the default values of *File Type* and *File Location*. Click **OK**.

Cr	reate Source File	8
Create a new s your project.	ource file and add it to	4
<u>F</u> ile type:	• Verilog	~
F <u>i</u> le name:		
Fil <u>e</u> location:	😜 <local project="" to=""></local>	~
?	0K Ca	ncel

Figure 17: Enter the new file name

The new file is added to the list of files of your project (Figure 18).

+, -	1.1.4					
	index	Name	Library	Location		
	1	adder.v	xi_defaultib	<local project="" to=""></local>		

Figure 18: Add Sources window with the new file added to the list

After you added and created the desired files click **Finish**.

Immediately after design source file or simulation source file creation, Vivado opens another dialog window (Figure 19) that allows you to define the interface for each newly created Design Source and Simulation Source. You may skip this option by clicking **OK**.

				Defin	ne Mo	dule	8
For	each port sp	ecified: alues will be	ignor	ed unle	ss its	your source file. Bus column is checked	. 🍌
Мо	odule Definit	ion					
	<u>M</u> odule name	e: adder					8
	I/O Port Def	initions					
	+  -	+   +					
	Port Name	Direction	Bus	MSB	LSB		
		input 🗸 🗸		0	0		
?	)					ок	Cancel

Figure 19: Define Module window

The interface of a module may be edited in the *I/O Port Definitions* table. For a single-bit port you should enter a *Port Name* and select its *Direction* (input by default). As an example, a newly created adder module is defined with 2 one-bit inputs a and b, and a third port, c, is declared as output. To change the *Direction*, click on the downward arrow and select the desired direction from the drop-down list (Figure 20).

				Defin	ie Mo	dule			(	×
For N	ine a module each port sp 4SB and LSB v Ports with blar	ecified: /alues will b	- be ignor	ed unle	ss its l			ecked.	4	
Mo	dule Definit	ion								
	<u>M</u> odule name	e: adder							8	
	I/O Port Def	initions								
	+ -	1 -								
	Port Name	Direction	Bus	MSB	LSB					
	а	input 💉	-	0	0					
	b	input 💉	/	0	0					
	с	input 🗸	· 🗌	0	0					
		input								
		outp					_		 	
?	)	inout						OK	Cancel	

Figure 20: Define module window, change a port direction

Some ports may have more than one bit. They may be defined by checking the *Bus* checkbox and entering the *MSB* and *LSB* values. *LSB* should be 0. *MSB* is equal to the desired width minus 1. The MSB and LSB values (default values are 0) may be changed by editing the *MSB* and *LSB* textbox or using the up and down arrows to increment or decrement the value.

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				Defin	e Mo	Jule			8
Fo	fine a module r each port sp MSB and LSB v Ports with blar	ecified: alues will be	ignor	ed unle	ss its l			ked.	A
м	odule Definit	ion							
	<u>M</u> odule name	e: adder							8
	I/O Port Def	initions							
	+   -	<b>t</b>   +							
	Port Name	Direction	Bus	MSB	LSB				
	а	input 🗸 🗸		0	0				
	b	input 🗸 🗸		0	0				
	с	output 🗸	$\checkmark$	1	0				
?	)						C	К	Cancel

Figure 21: Define module window, change a port width

Click **OK**. To finish file creation.

- Each module is in a separate source file.
- The name of the source file is the name of the module.
- Keep the default file location for any created file.
- The top-level module name and its source file name must match the name of the project.

# Add Source Files

If you want to include in your project a file that is already on your computer open the *Add Sources* window as shown in the previous section and click **Add Files** button (Figure 22):

Add Sources		
Add or Create Design Sources Specify HDL nelist. Block Design, and IP files, or direc life on disk and add if to your project.	dories containing those the types to add to your project. Create a new source	2
+, - : :		
1268 8457	las, Add Directories or Disally File Suffers better	
dds File	Ags Directories Greate File	

Figure 22: Add Sources window.

A file browser opens (Figure 23). Use the 'Up' button (encircled in red) to go up in the file hierarchy and click on folder names in the left panel to go down in the file hierarchy. Select the files you want to copy into the project and click **OK**.

ok in: 🔐 andther project	- 🕐 = = = = = = = = = = = = = = = = = =
9 wilder v	Recent Directories
	C Assensatudent 🗸
	file Preview
	timescul in / ips // Emproyr // Employr // Employr // Erests Date: 23.07.0027 18150188 // Decays None: // Decays None: // Perject Decays adder // Perject Name! // Perject Name! // Perject Name! // Decays Decays // Perject Name! // Decays Decays // Perject Name!
	1 m 5
e game adder.v	
	who, v, vt veriling, vr, vp, vb, ft, vlog, vp, vm, veo; svo, vh, h, svh, vhp, avhp, edh, edit, edit, ngc, sx, svp, bmm, mit, mem

Figure 23: Add Source File browser

The selected files are added to the list of project files in the *Add Sources* window (Figure 24). You should check the *Copy sources into project* checkbox. Click **Finish**.

+,	-	1 1			
	index.	Name	Library	Location	
e.	1	adderv	xil_defaulfilb	C/Users/student/another project	
			ſ	Add Files Add Directories Crieste File	
			[	Add Files Qreate File	

#### Figure 24: Add Sources window

• Make sure that any added file is also copied into project.

# Source File Editor

To open a file for editing double click the file in the *Sources* panel. The editor window (Figure 25) opens in another tab of the rightmost panel of the Vivado Project window. You may edit all the file.

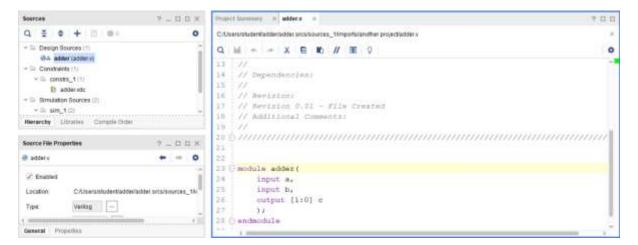


Figure 25: File editor window

To save the file click on the 'Save' icon at the top row of the editor window. After a file is changed and saved, Vivado updates the hierarchy of modules in the *Sources* panel (this takes a few seconds).

## Simulation

On the left panel *Flow Navigator* expand the SIMULATION section and click on **Run Simulation**. From the pop-up menu list select **Run Behavioral Simulation**. Vivado starts the elaboration of the design. This takes some time while a dialog shows the progress of this compilation:

nun Simulation	
Executing elaborate step	
	International Accession

If the elaboration succeeds, Vivado opens the Simulation window (Figure 26).

scope × biarrow		- 0.0	Objects		7 _ B B X	Civilled 2					700
9 I 0		0	Q		0	Q M Q Q	22 - 14	Histo	r f fa i	4141	
iame	Design U.	Black Type	Name	Value	Date T.					1,00	0,000 pm
W adder_B	80094_32	Verlog M.	10 a	<u>0</u>	Lopic	Name	Value	(1993, 597 ye)	1888, 888 p.e.	1000,000 pm	1,200,000
Set Set	20301	Verlog M.,	16.5	0	Lopic		0	222,227 pt	222,000 Be	227,772 28	11200730
🖬 gibi	gts:	Verling M.	A 46 (\$1.0)	0	Acray .		0				
						1 10 41.00	a .		2.6		
					2						
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. ∓ + II		8									? <u>-</u> 0
11 0 I 0 1	E I	mpleted. Des	Em stapsbor fad	ns_th_before* 1	aded.			-			
1 = 0    1070- (797-654 1070- (797-654	-H4) 131m c	B impleted. Des inclation res	for 1000mm					. 2			? <sub>-</sub> 0
1 2 0 II 1070- (797-604 1070- (797-604	-H4) 131m c	B impleted. Des inclation res	for 1000mm			190,145 ž gain = 0,00					
1 2 0 II 1070- (797-604 1070- (797-604	-H4) 131m c	B impleted. Des inclation res	for 1000mm			190,149 i gain = 0.00		-			

Figure 26: Vivado Simulation window

The Simulation window has four panels. The leftmost *Scope* panel shows the hierarchy of the modules instantiated in your project, with the testbench module at the root of the hierarchy. The middle *Objects* panel lists all signals for the module that is selected in the *Scope* hierarchy. The rightmost panel draws the waveforms of the signals chosen to be displayed. By default the Simulation window opens with the testbench module selected and with all its signals been displayed on the waveform panel.

The bottom panel (*Transcript* panel) reports messages from Vivado and logs everything displayed by the simulated modules themselves.

The most important controls of the simulation are the **Restart**, **Run All** and **Relaunch Simulation**. They are available from Vivado main menu **Run** section but are easier to choose from Vivado toolbar (Figure 27).



Figure 27: Vivado Simulation controls

The Wave window may be arranged to suit your needs. You may rearrange the signals by clicking a signal name and dragging it up or down in the list. You may shrink or expand the time scale using the **Zoom In**, **Zoom Out** and **Zoom Fit** icons of the Wave window's toolbar (Figure 28).

Z	oom In	Zoom Out	Zoom Fit	?
	- 00 A	Untitled 2		7 D D X
	0	Q # Q Q X *	H 🖬 🛫 📲 🕞 🗐 🗐	0
Value	Data T.		525,378 pt	
1	1 most			

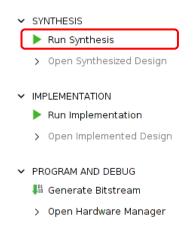
Figure 28: Wave window main controls

**Note**: If there are no signals in the Wave and Object windows, that means the testbench has not compiled because of compiling errors, or it has not loaded because the module it instantiates does not match the compiled top-level design module (the interface is different, or the module name does not match). In the *Scope* panel at the left of the Simulation window you will see some instances, but not the testbench instance. In that case you must look for the errors in the *Transcript* panel at the bottom of the simulation window, close the simulator, fix the errors in the testbench, and then relaunch the simulator.

# I/O Ports Assignment

# Synthesis and Implementation

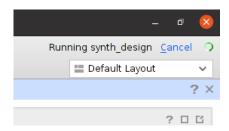
On Flow Navigator panel expand the SYNTHESIS section and click on Run Synthesis.



In the dialog window that appears keep all default settings and click **OK**.

Launci	h Runs 💈
Launch the selected synthesis or impl	ementation runs.
Launch <u>d</u> irectory: 📮 <default laun<br="">Options</default>	ch Directory> 🗸 🗸
Launch runs on local host:	Number of jobs: 2 🗸
O Launch <u>r</u> uns on remote hosts	Configure <u>H</u> osts
🔿 Launch run <u>s</u> on Cluster	lsf 🗸 🗸
○ <u>G</u> enerate scripts only	
Don't show this dialog again	OK Cancel

The synthesis takes some time to complete (between tens of seconds and tens of minutes, depending on the design complexity and constraints). While it is running the message Running synth\_design appears at the top-right corner of the main program window:



When the synthesis finishes a dialog window appears:

Synthesis Completed 🛛 💈	3
<b>i</b> Synthesis successfully completed.	
Next	
<u>Run Implementation</u>	
Open Synthesized Design	
○ View Reports	
Don't show this dialog again	
OK Cancel	

Keep the default choice (Run Implementation) and click **OK**.

In the new dialog window that appears keep all default settings and click **OK**.

Launc	h Runs 😣
Launch the selected synthesis or impl	ementation runs.
Launch <u>d</u> irectory: 📑 <default laun<br="">Options</default>	ch Directory> 🗸
-	Number of jobs: 2
Launch runs on local host:	
Launch <u>r</u> uns on remote hosts	Configure <u>H</u> osts
🔵 Launch run <u>s</u> on Cluster	lsf 🗸
Generate scripts only	
Don't show this dialog again	OK Cancel

The implementation is also a time-consuming process, even more so than the synthesis. While it is running a info message appears at the top-right corner of the program's main window. If the implementation finishes without errors a dialog window opens:

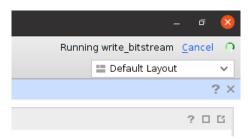
	Implemen	tation Comp	leted	×
i Im Next	plementation	successfully	completed.	
0	pen Implemer	nted Design		
<u> </u>	enerate Bitsti	ream		
⊙⊻	iew Reports			
<u>D</u> on'	t show this di	alog again		
		ОК	Cancel	

Keep the default choice (Generate Bitstream) and click OK.

In the dialog window that appears keep all default settings and click **OK**.

Launci	h Runs 🙁
Launch the selected synthesis or impl bitstream.	ementation runs and generate 🗼
Launch <u>d</u> irectory: 🕞 <default laun<="" th=""><th>ch Directory&gt; 🗸</th></default>	ch Directory> 🗸
Options	
Launch runs on local host:	Number of jobs: 2 🗸 🗸
○ Launch <u>r</u> uns on remote hosts	Configure <u>H</u> osts
🔘 Launch run <u>s</u> on Cluster	lsf 🗸
O Generate scripts only	
□ D <u>o</u> n't show this dialog again	
	OK Cancel

The bitstream generation also takes some time, while an info message is displayed at the top-right corner of the program main window:



If the bitstream generation finishes without errors, another dialog window opens up:

Bitstream Generation Completed	8
<b>i</b> Bitstream Generation successfully completed.	
Open Implemented Design	
○ View Reports	
💿 Open <u>H</u> ardware Manager	
O Generate Memory Configuration File	
Don't show this dialog again	
OK	

Keep the default choice (Open Hardware Manager) and click OK.

# Device Programming

If the board is not powered up the following message appears above the central panel:

HARDWARE MANA	GER - unconnec	ted	
🚯 No hardware tar	get is open. <mark>Op</mark> e	en target	
Hardware		? _ 🗆	ц×
0,   ≚   ≑   4	3   <b>&gt;</b>   <b>&gt;</b>   I		Ф
	No content		

Power-up the Pynq-Z2 board, then click **Open target**. From the drop-down menu click on **Auto Connect**:

Recent Targets	Hardware		Auto Connect	
Q       I ⇒       I ⇒       I ⇒       Available Targets on Server         Open New Target			Available Targets on Server 🕨	

If the board is power-up and connected to the computer, the following list appears in the Hardware panel:

HARDWARE MANAGER - localhost/xilin>	_tcf/Xilinx/123
There are no debug cores. Program	device Refre
Hardware ?	_ 🗆 🗆 ×
Q   素   ♦   ∅   ▶   ≫   ■	•
Name	Status
✓ 【 localhost (1)	Connected
✓ ■ ✓ xilinx_tcf/Xilinx/1234-tulA (2)	Open
🛑 arm_dap_0 (0)	N/A
✓ ⊕ xc7z020_1 (1)	Not program
1 XADC (System Monitor)	
<	

It shows that the localhost (your computer) is connected to a Xilinx chip which has an ARM processor and an FPGA. Click on the FPGA **xc7z020** and in the pop-up window that shows-up click on **Program Device** ...

HARDWARE MANAGE	<b>R</b> -	ocalhost/xilin	_tcf/Xilinx/123	34-t	ulA	
🚯 There are no debug	g co	res. Program	device Refre	sh	device	
Hardware		?	_ 🗆 🖒 ×		adder.v × adder	
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🗸 🚺 localhost (1)			Connected		1 timescale lns	
✓ ■	nx/1	234-tulA (2)	Open			
arm_dap_0	(0)		N/A		3 // Company:	
∨ @ xc7z020_`	(1)	Llandurana Da			4 ; // Engineer:	
I XADC (		Hardware De	vice Propertie	es	. Ctrl+E	
		Program Dev	ice			
		Verify Device				
	С	Refresh Device				
		Show Bus Plo	ot			
٠		Add Configur	ation Memory	De	vice	

A dialog window appears, allowing you to select the bitstream file to be written into the target device. If you followed the above default steps, keep the default *Bitstream file* selection and click **Program**.

	Program Device 🛛 😵
can optionally select	ogramming file and download it to your hardware device. You a debug probes file that corresponds to the debug cores ream programming file.
Bitstre <u>a</u> m file: Debu <u>g</u> probes file: ✔ <u>E</u> nable end of s	
<b>?</b>	<u>P</u> rogram Cancel

If the target device (the FPGA or the board) was correctly set up during the project initialization, the bitstream could be written into the FPGA, and the PL programming "done" LED should be on.

Your project is ready to use.

# Quick Project Guide

• New Project wizard

0

- Step 1 (Project Name)
  - **Project name**: *myProject*
  - Check Create project subdirectory checkbox
- Step 2 (Project Type)
  - Select RTL Project
  - Step 3 (Add Sources)
    - Skip this step: Select OK
- Step 4 (Add Constraints)
  - Skip this step: Select OK
- Step 5 (Default Part)
  - Change tab to **Boards**
  - From Boards list select the *pynq-z2* board
- Create source files
  - Click 'Plus' on *Sources* panel
  - Choose file type, then Next
  - o Click Create File on Add Sources dialog, then Next
  - o Click Finish in the Add Sources dialog
  - Optionally edit the interface. Otherwise let it unfilled and click **OK**.
- Add source files
  - Click 'Plus' on Sources panel
  - Choose file type, then **Next**
  - Click Add File on Add Sources dialog
  - Select the desired file, then **OK**
  - o Click Finish in the Add Sources dialog
- Flow Navigator -> SIMULATION -> Run Simulation -> Run Behavioral Simulation
- Flow Navigator -> SYNTHESIS -> Run Synthesis
- Flow Navigator -> IMPLEMENTATION -> Run Implementation
- Flow Navigator -> PROGRAM AND DEBUG -> Generate Bitstream
- Flow Navigator -> PROGRAM AND DEBUG -> Open Hardware Manager
  - $\circ$  Power on the physical board (the 'power on' red LED should be on)
  - Open target -> Auto Connect
  - o XC7Z020 -> Program Device ...
  - Keep the default *Bitstream file* name and click **Program**