Sine wave signal generator
-functional description-

It is required to design a sine wave signal generator with the following characteristics:

- The oscillation frequency has a fixed value of f=3.18KHz;
- The amplitude of the output signal is 12V peak to peak (p-p);
- The output load is 50 ohm;
- The signal generator should have the positive feedback circuit as the Wein type.

A possible impementation by using discrete components is presented in Fig. 1.

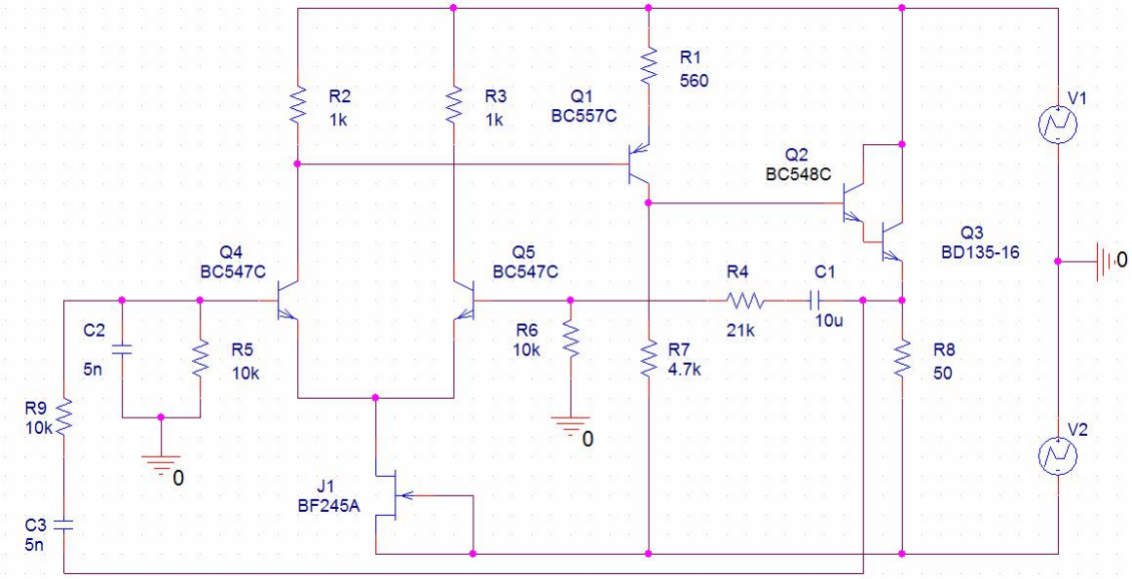

Fig 1. The schematic diagram of the sine wave signal generator

As it may be observed, the sine wave signal generator consists of:

1. a positive feedback circuit formed with the Wein C3-R9-C2-R5 network that determines the oscillation frequency expression from the Barkhausen stability criterion for sustained oscillations:

$$f = \frac{1}{2 \cdot p \cdot R \cdot C}$$

because the network has equal elements;

2. a negative feedback circuit formed by the R6-R4 network (a voltage divider);

3. an open loop amplifier based on 5 small signal silicon transistors (J1, Q4, Q5, Q1, Q2) and one medium power bipolar junction transistor (Q3);

4. two power supply units ($V_{1.2}$= 10V).

The circuit is a low frequency amplifier made entirely of bipolar transistors of European production with a series-shunt (series voltage) negative feedback. The load resistance of the amplifier is R8.

The input stage (Q4-Q5) is a classic differential amplifier made by small signal bipolar junction transistors. It may be observed that a constant-current source based on a junction field effect transistor (JFET) is mounted in the emitters of the transistors which form the differential amplifier. The current source determines a collector current of 2mA through each transistor which forms the differential amplifier (I_{C4} = I_{C5} = 2mA).

The differential asymmetric stage is followed by a distributed load amplifier (Q1) which it usesa low-power (300mW) high-gain (h_{femin} = 420) bipolar junction transistor. The collector current of Q1 (approximately 2mA) is assured by biasing the base-emiter junction through R1-R2 and it is influenced by I_{C4} . The current gain of the circuit is performed with the pair Q2-Q3, which forms a Darlington amplifier. The C1 capacitor is mounted to allow only AC signals through the negative feedback circuit.

The load resistance (R8) is directly connected to the emiter follower amplifier (Q3). The output is not protected against short-circuit. This can still be done by using a 500mA fuse mounted in series in the supply line, or electronically, by using a circuit to monitor the collector current of the final stage. The Q3 transistor should be mounted on an aluminum heatsink painted in black.

The global gain of the negative feedback amplifier circuit is approximately:

$$A_V = 1 + \frac{R_4}{R_6}$$

Suggestion regarding the negative feedback amplifier:it is required to calculate the DC bias of the circuit, to draw the equivalent AC –small signal circuit, to compute the open loop gain and the power dissipated by the output stage, dimensionning accordingly the heatsink. The non-destructive biasing of the Darlington circuit should be be demonstrated.