Circuite integrate digitale

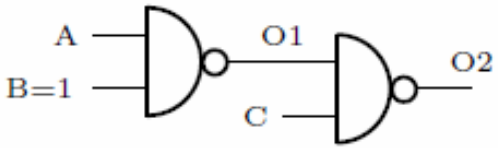
Curs 6

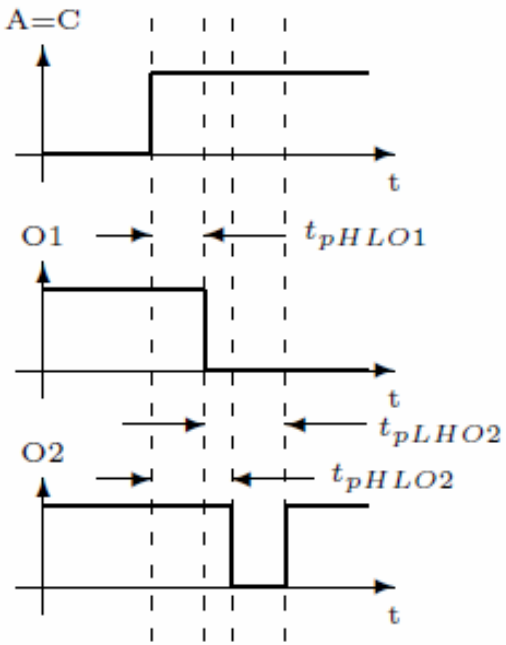
Curs 6

- hazard
- circuite CMOS (continuare):
  - multiplexor
  - latch-uri
- circuite logice programabile
- ROM
- RAM
- numărătorul

Hazard

- A şi C comută din 0 în 1
- ieşirea ar trebui să fie 1 tot timpul
- denumiri uzuale:
  - *glitch*
  - *spike*



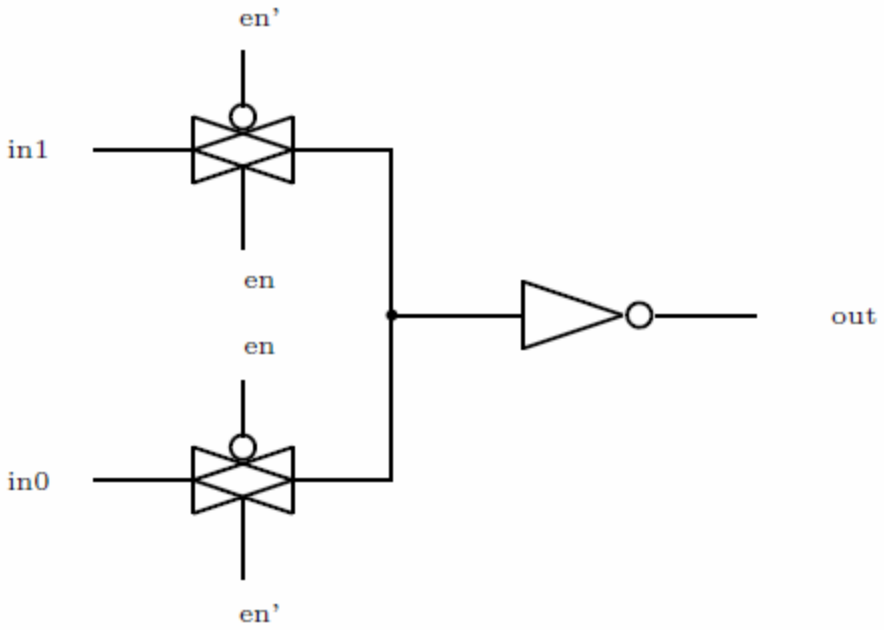


Hazard

- Comportament neideal al circuitelor digitale
- Dezavantaje:
  - poate fi memorat (blocat printr-un latch)
  - consum de putere

- Semnalele de comandă nu au voie să aibă hazard

Multiplexor elementar inversor

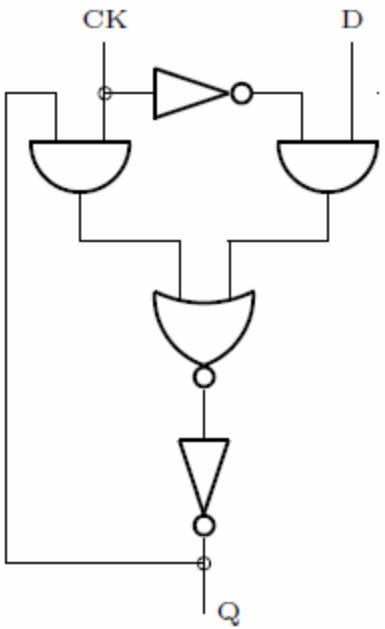


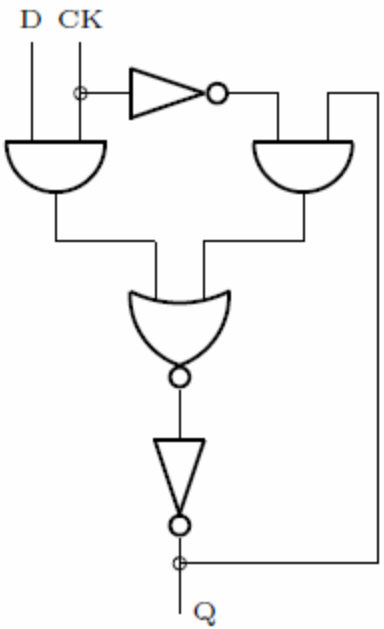
putere mică, arie redusă, viteză mică

Circuite de memorare

- Latch-uri D (data)
- Bistabilul D (delay flip-flop (DF-F)
- Bistabil D resetabil

Latch-uri D

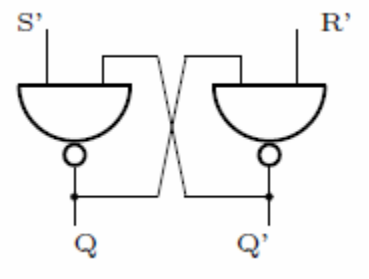


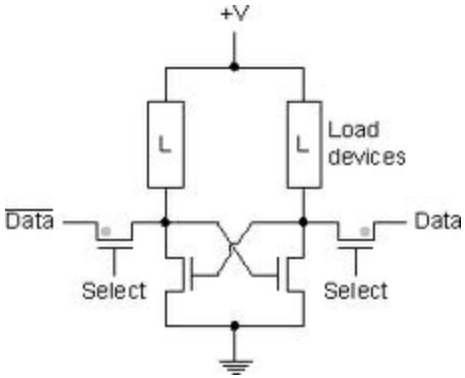


0 : palier activ al CK
CK = 1 : bucla inchisa
CK = 0 : transparent

1 : palier activ al CK
CK = 1 : transparent
CK = 0 : bucla inchisa

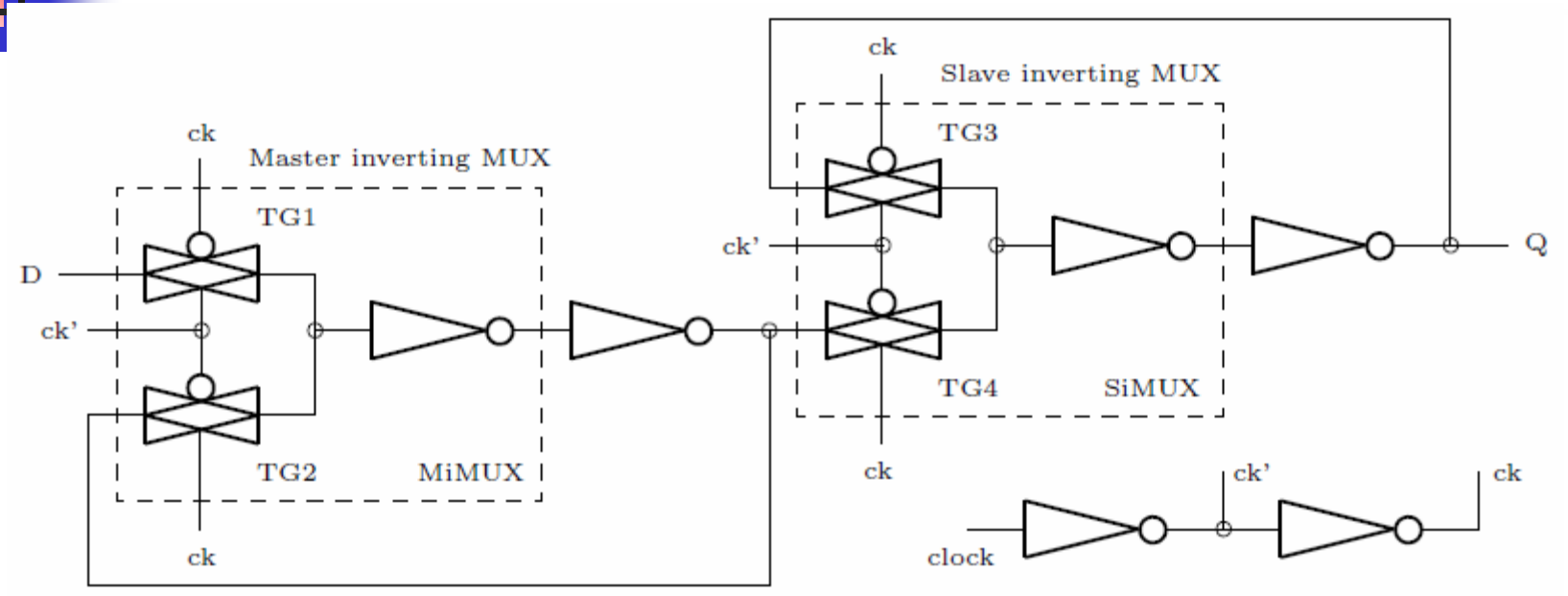
Latch elementar





- schemele anterioare nu implementează latch-ul elementar
- latch cu inversoare – celula de memorare SRAM

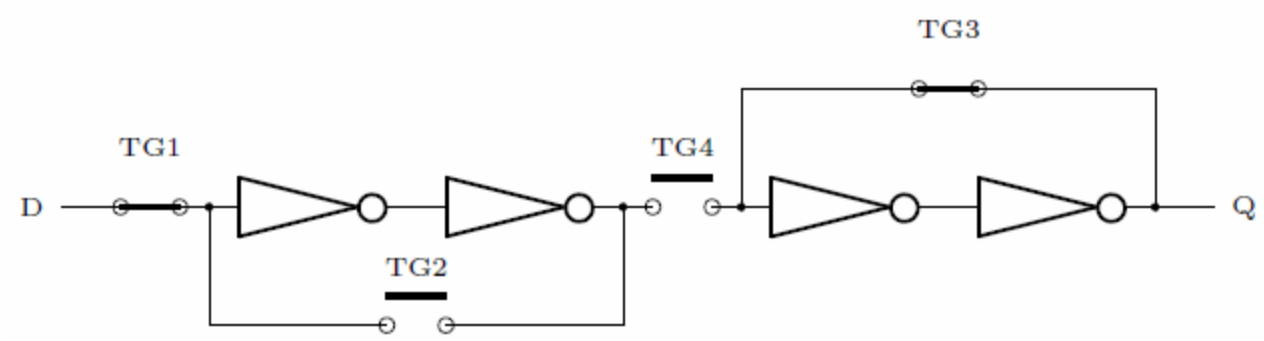
Structura master-slave a bistabilului D



- Care este frontul activ al semnalului de ceas?
- Cum poate fi modificat?

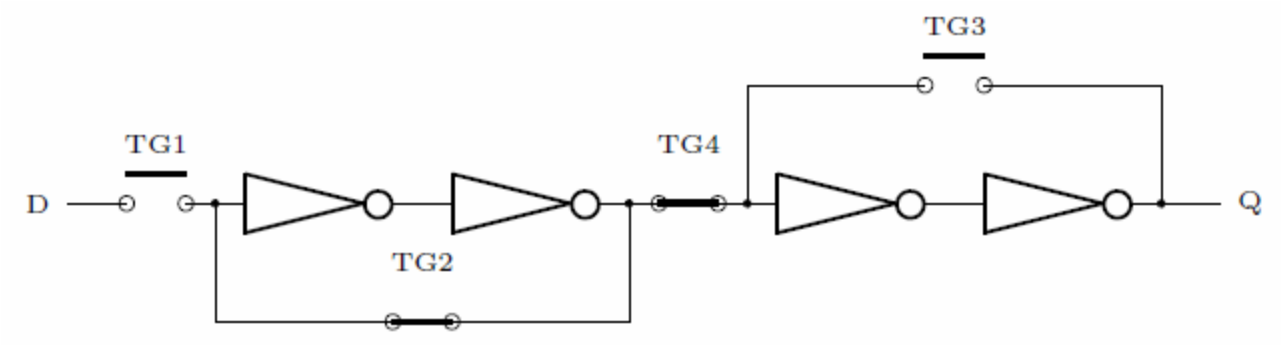
Funcţionarea bistabilului D (1)

- Latchul master este transparent,
- Latchul slave este blocat

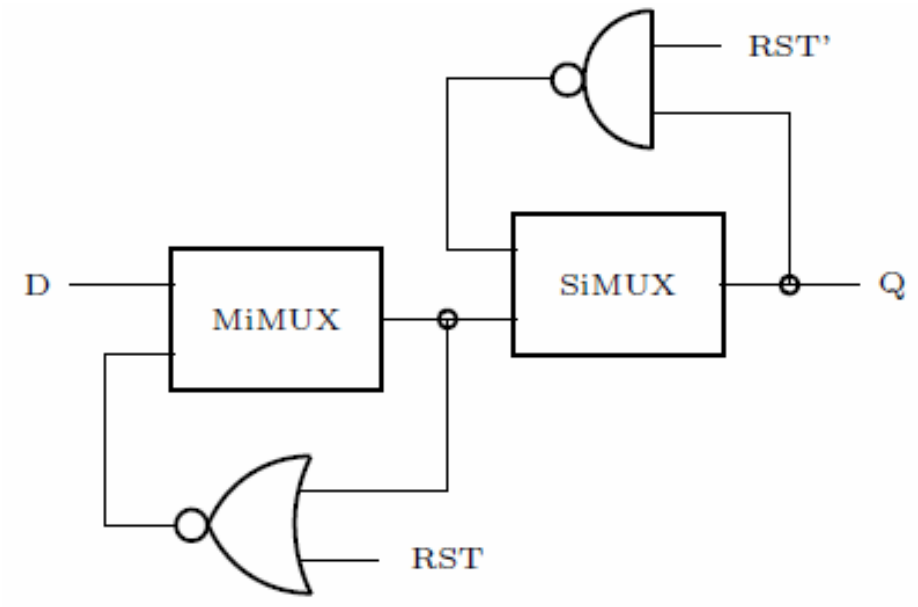


Funcţionarea bistabilului D (2)

- Latch-ul master este blocat,
- Latch-ul slave este transparent
- structura de ansamblu nu este transparentă niciodată



Bistabil D resetabil – tema 7

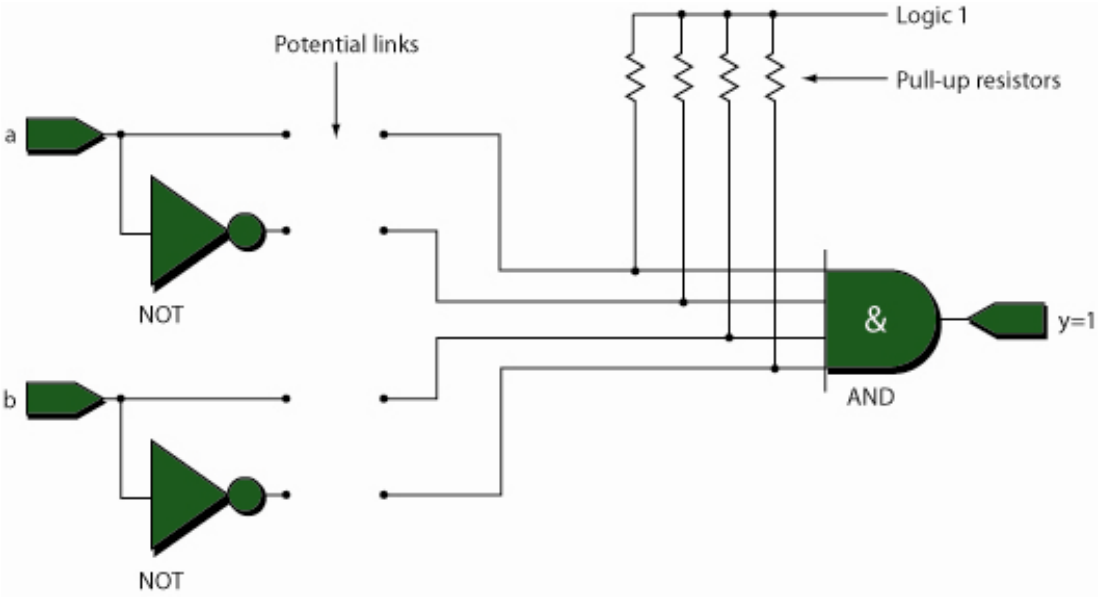


- Desenaţi schema cu tranzistoare
- explicaţi funcţionarea circuitului

Dispozitive logice programabile

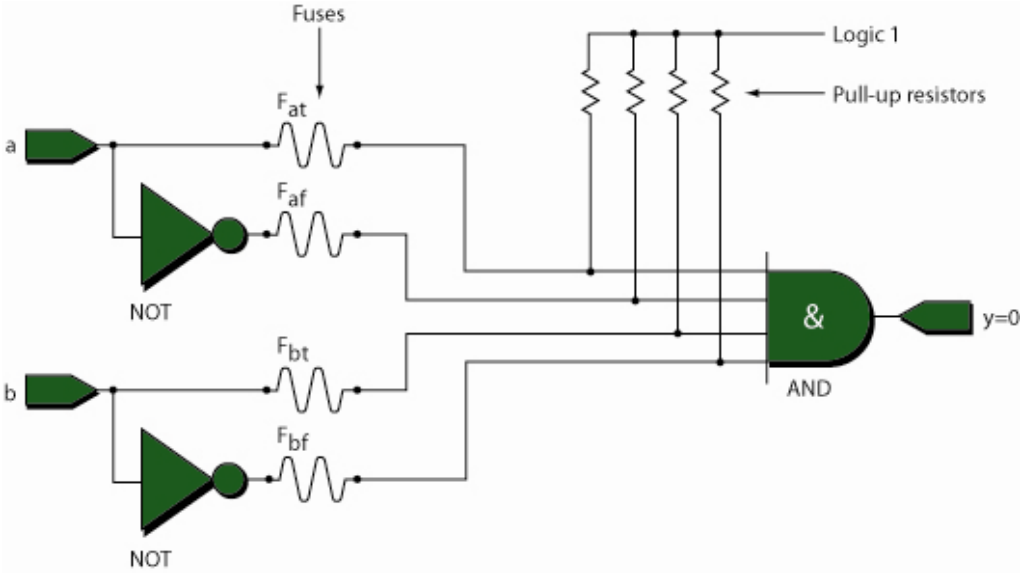
- circuite combinaţionale care pot implementa diferite funcţii, folosind aceleaşi porţi logice
- programarea înseamnă **configurare**
- se bazează pe scrierea funcţiilor logice ca sumă de produse (SOP – *sum of products*)

Principiul logicii programabile

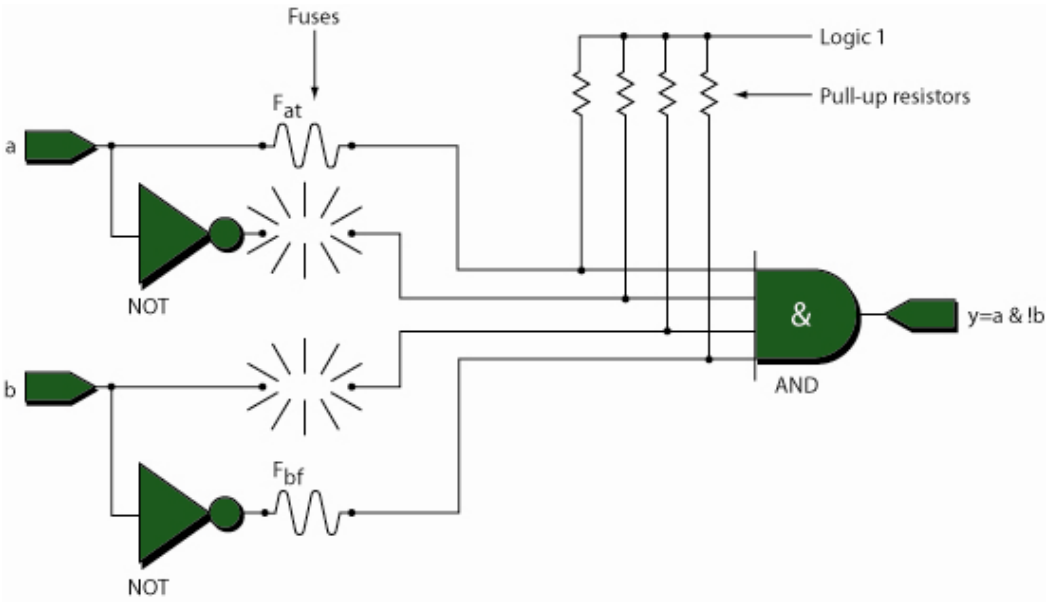


- în funcţie de conexiunile pe care le facem, se implementează diferite funcţii

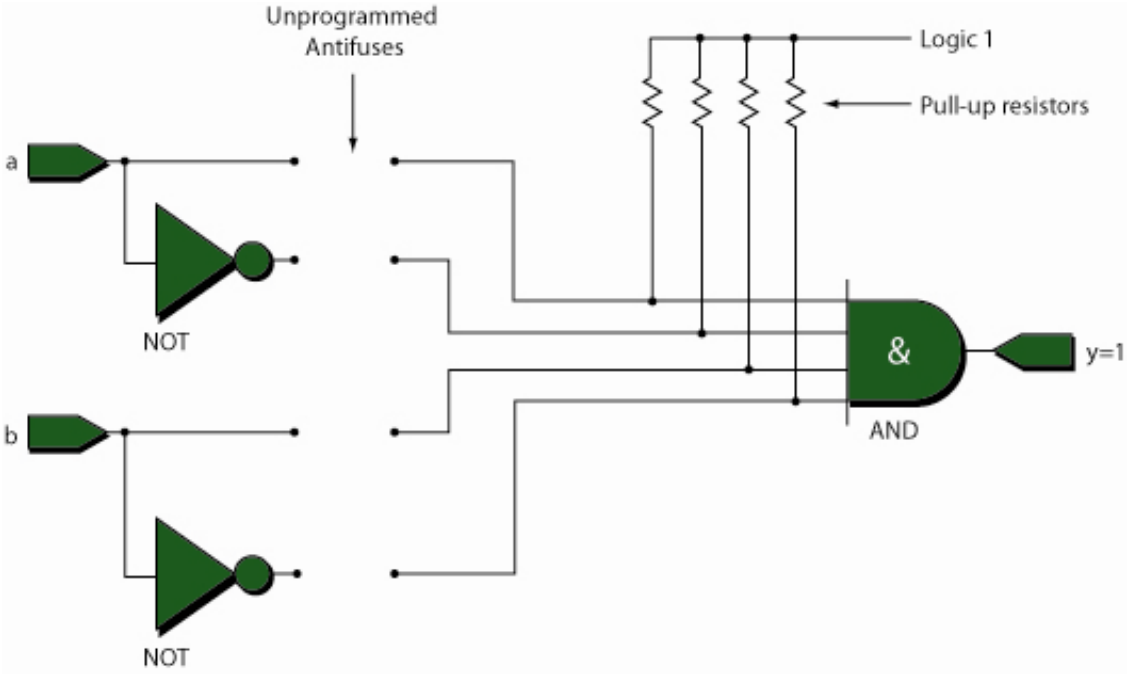
- în realitate, cel mai simplu – tehnologic – este să aplicăm acest principiu exact pe dos

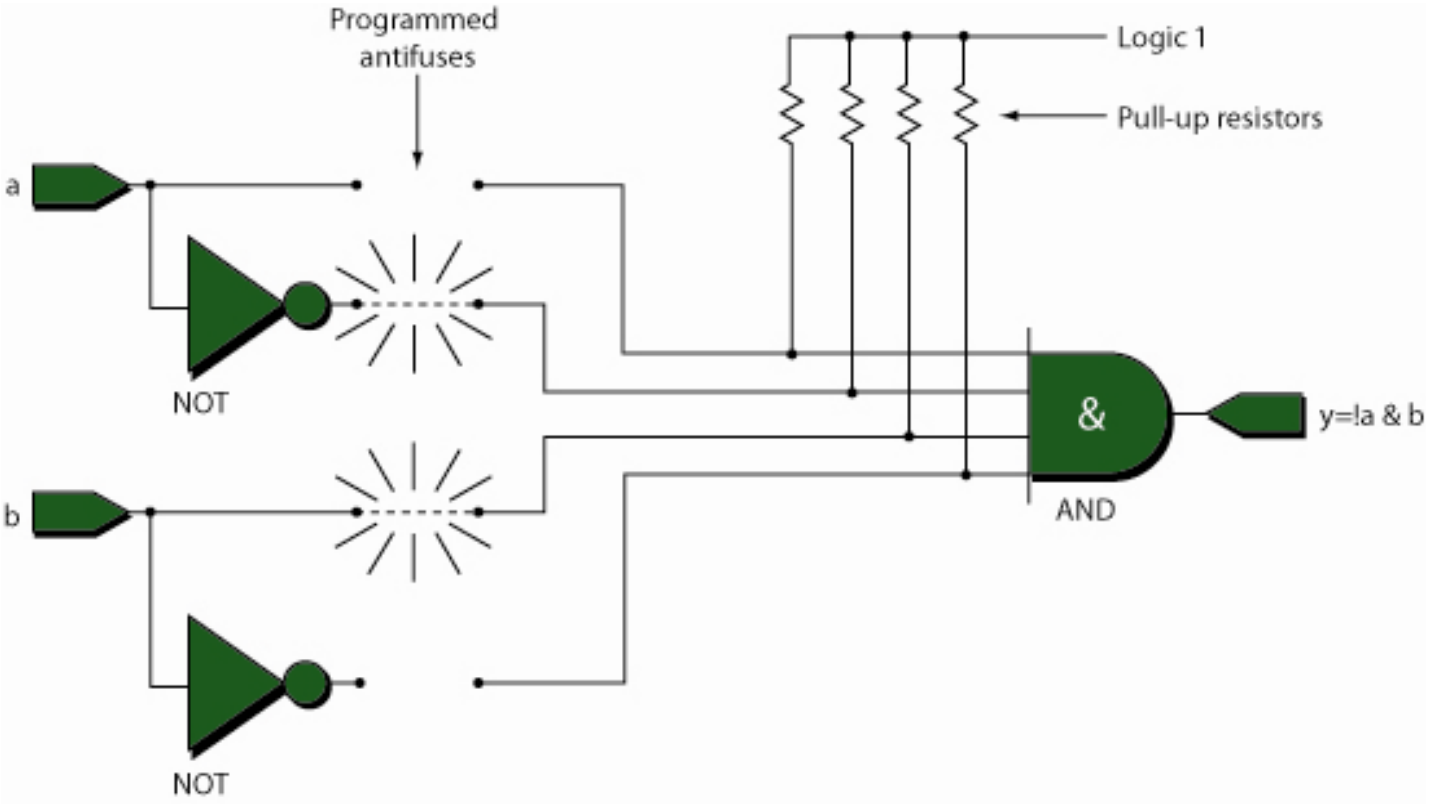


- Programarea = arderea rezistenţelor fuzibile (este destructivă)

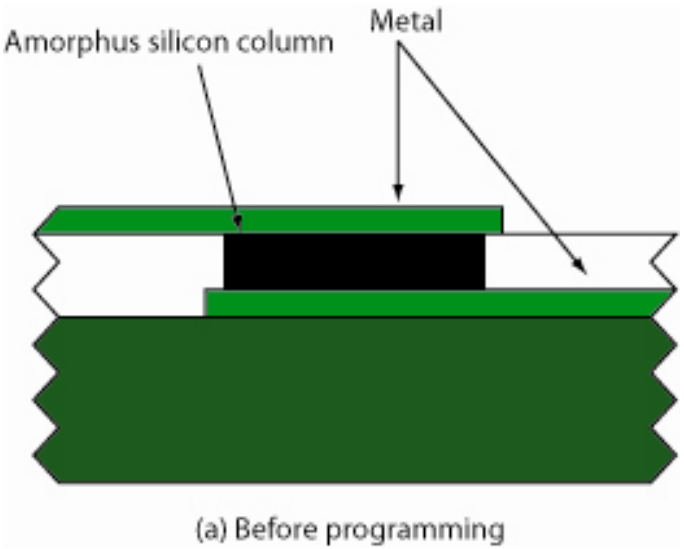


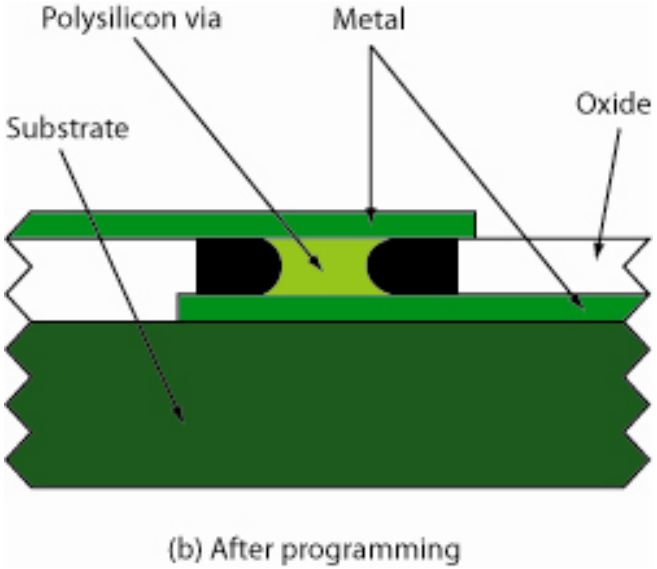
- Există şi o tehnologie care implementează direct principiul conectării programabile!




Programmed
antifuses
Logic 1
Pull-up resistors
a
NOT
b
NOT
&
AND
y=!a & b

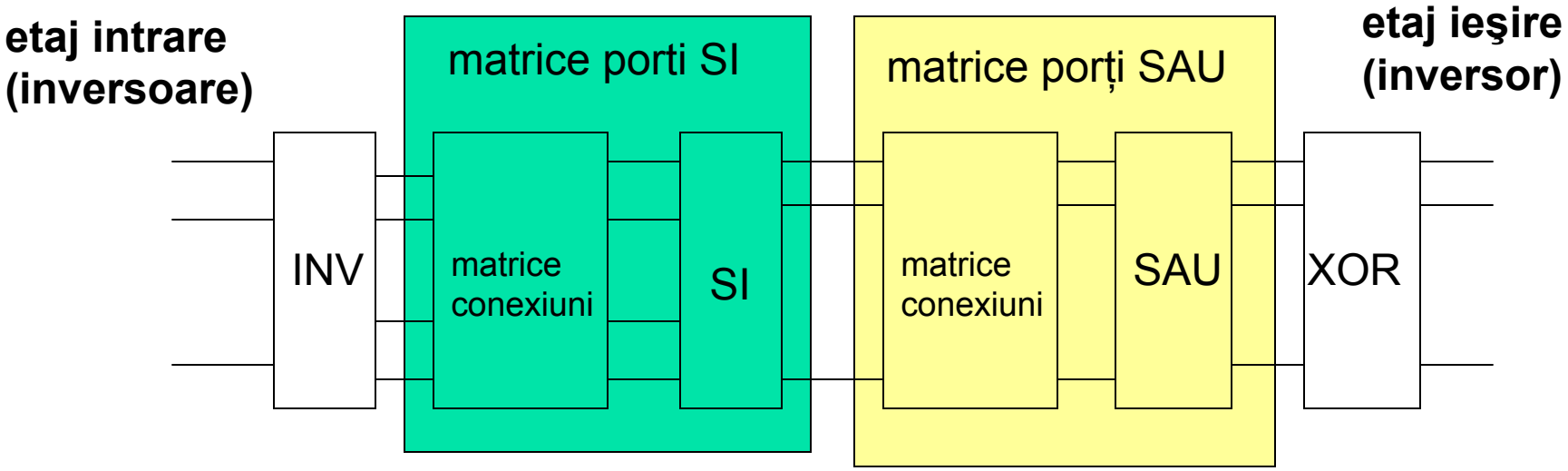
Antifuse


Amorphus silicon column
Metal
(a) Before programming


Polysilicon via
Metal
Substrate
Oxide
(b) After programming

PLD

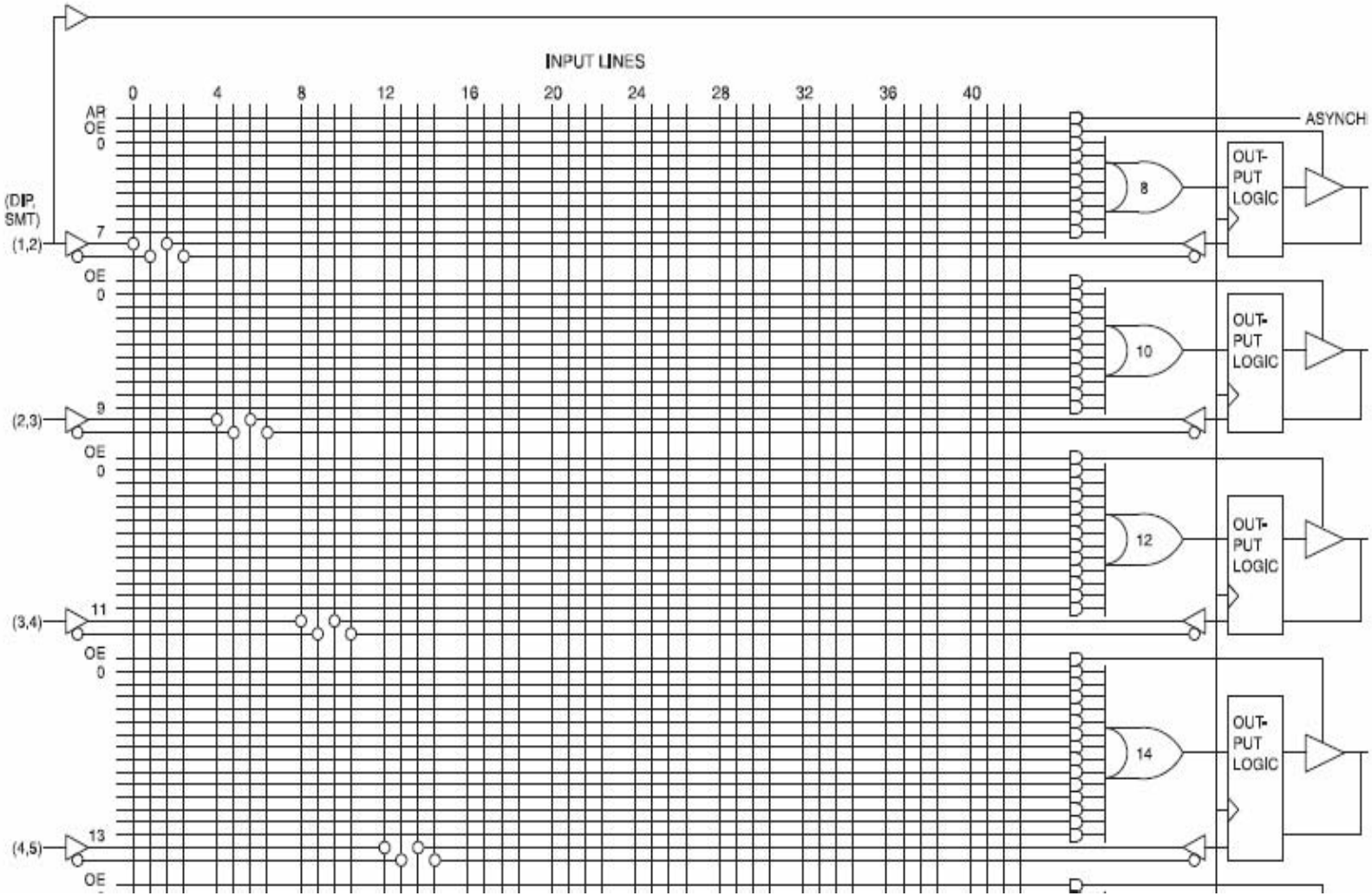
- dispozitive logice programabile (se “programează” conexiunile)



Tipuri de PLD-uri

	matrice SI	matrice SAU
ROM	fixă (DCD) maximă	programabilă
PLA	programabilă	programabilă
PAL	programabilă	fixă

11. Functional Logic Diagram

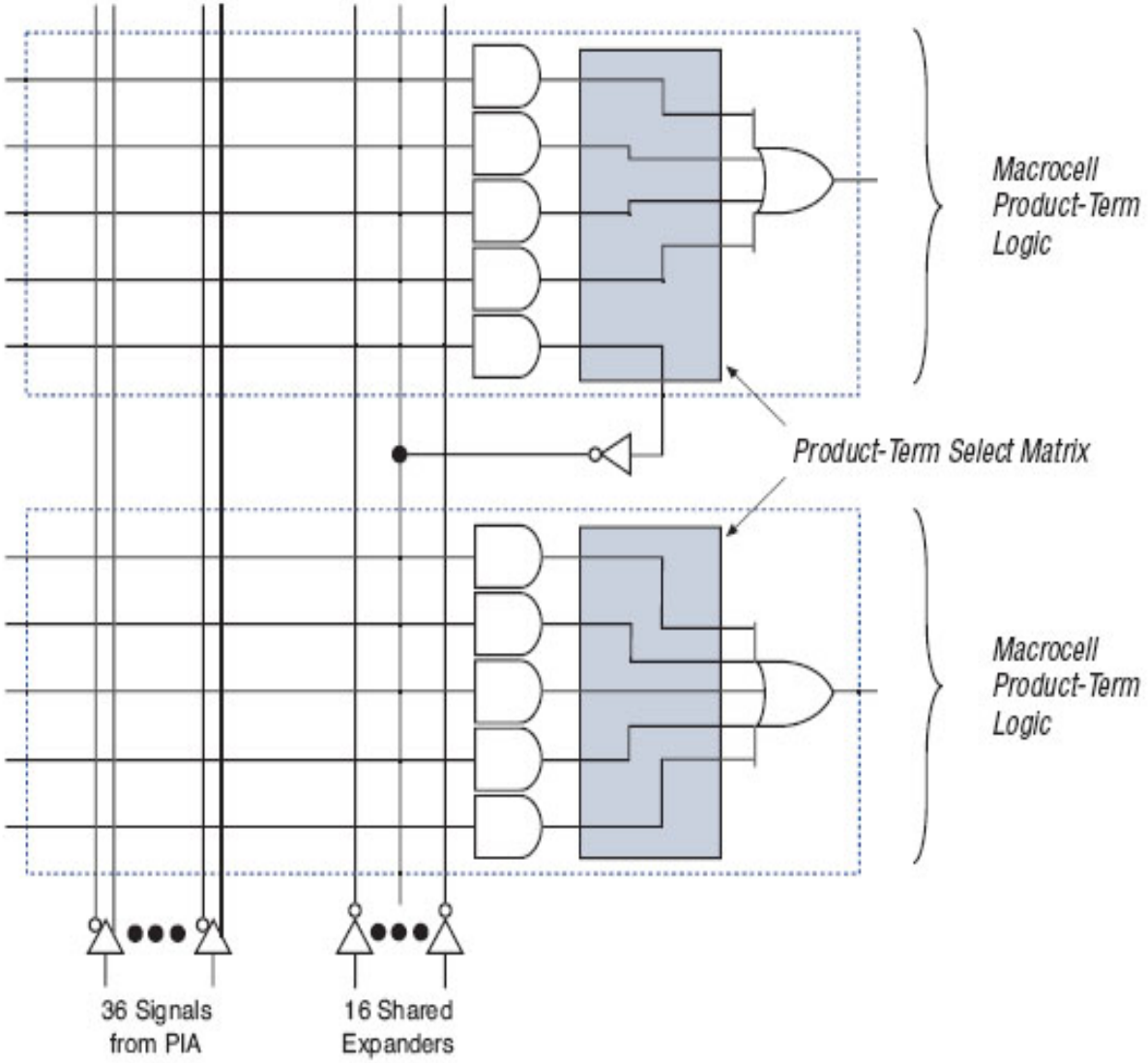


CPLD

- Complex Programmable Logic Device
- dispozitiv logic programabil cu complexitate intermediară între PLD şi FPGA
  - PLD: programmable logic device
  - FPGA: field programmable gate array
- elemente de structură de la PLD şi FPGA

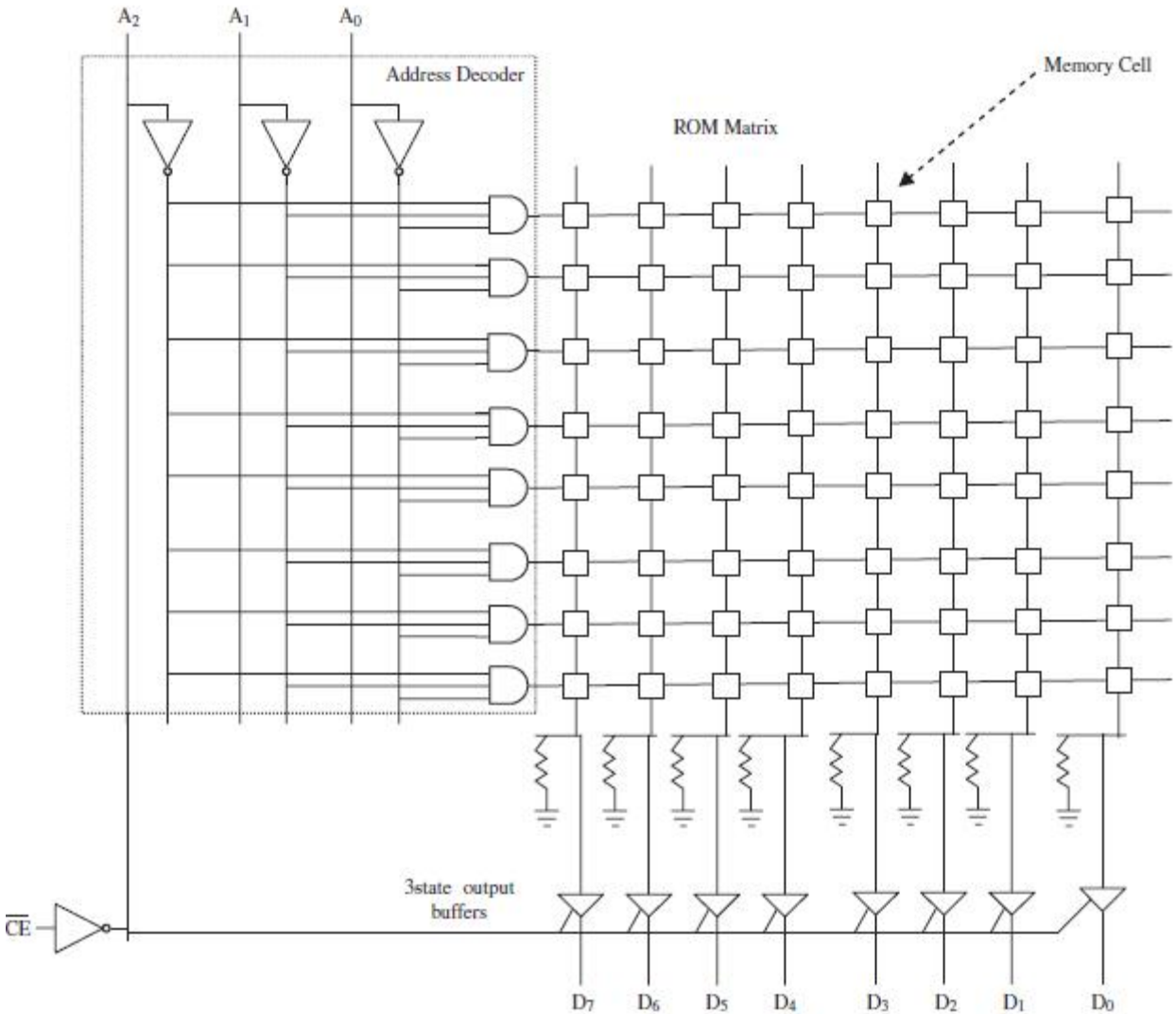
MAX 3000A Shareable Expanders

Shareable expanders can be shared by any or all macrocells in an LAB.



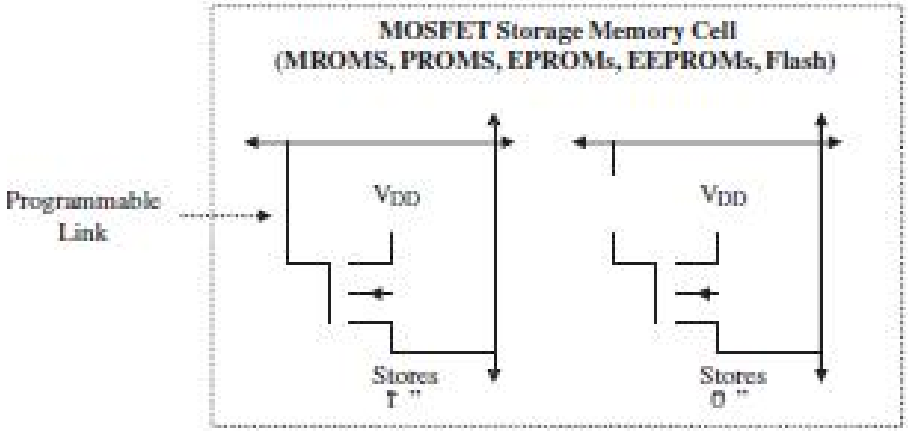
ROM

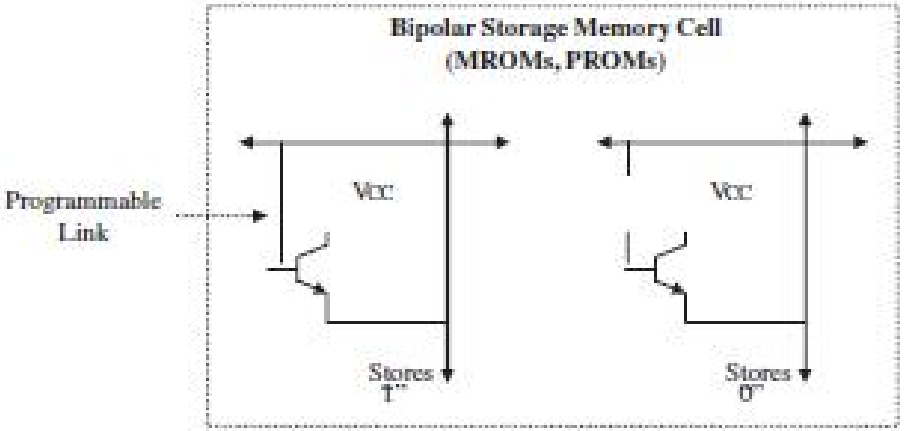
- Read Only Memory
- circuit combinaţional (SO0), adică nu este o memorie propriu-zisă


A2
A1
A0
Address Decoder
Memory Cell
ROM Matrix
3state output
buffers
CE
D7
D6
D5
D4
D3
D2
D1
D0

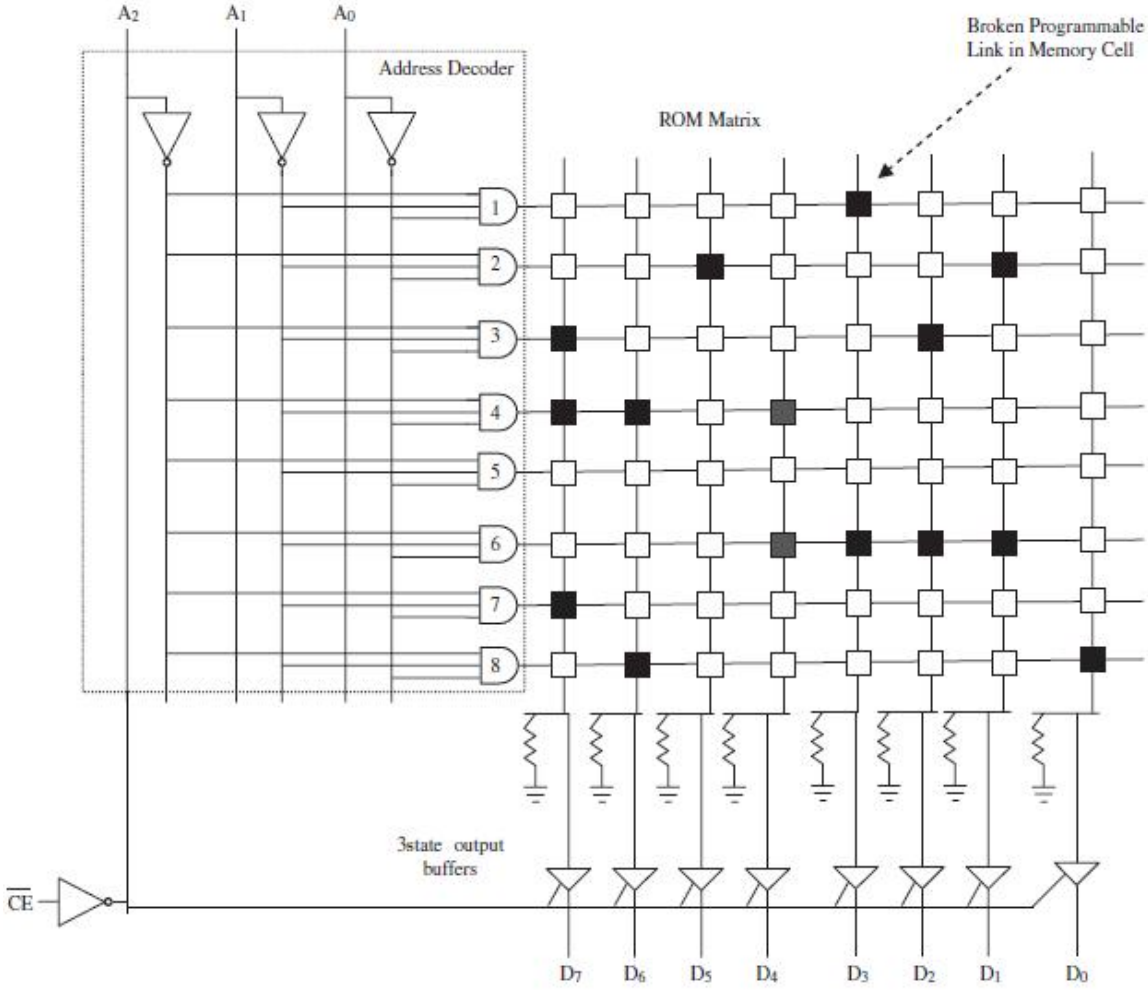
Celulele de memorie ROM

- sunt conexiuni programabile





Gate	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	1	1	1	1	0	1	1	1
2	0	0	1	1	1	0	1	1	1	0	1
3	0	1	0	0	1	1	1	1	0	1	1
4	0	1	1	0	0	1	0	1	1	1	1
5	1	0	0	1	1	1	1	1	1	1	1
6	1	0	1	1	1	1	0	0	0	0	1
7	1	1	0	0	1	1	1	1	1	1	1
8	1	1	1	1	0	1	1	1	1	1	0



Tipuri de ROM

- care sunt deja programate de producător în fabrică (cu măşti - MROM) /pe care le poate programa utilizatorul (PROM) folosind un aparat special (PROM programmer sau burner)

- PROM - programmable ROM
  - care se pot programa o singură dată (OTP)
  - care pot fi "şterse" şi programate din nou (EPROM) – optic
  - EEPROM – electrically erasable PROM
  - memorii flash – ştergere şi rescriere în blocuri

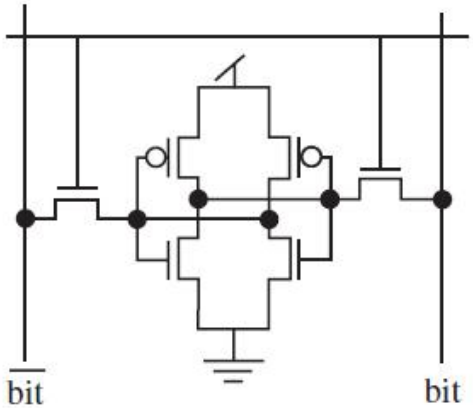
RAM

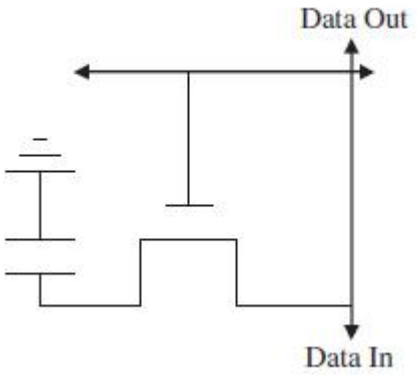
- Random Acces Memory
- diferenţa faţă de EEPROM este că se poate accesa orice locaţie, oricând în timpul folosirii

TERMENI

- memorie *volatilă* – care se şterge când circuitul nu mai este alimentat (*nonvolatilă* – care nu se şterge…)
- care poate fi ştearsă-rescrisă: *erasable (non-erasable*: memorie care nu poate fi rescrisă)

Celule de memorie RAM





RAM static

SRAM

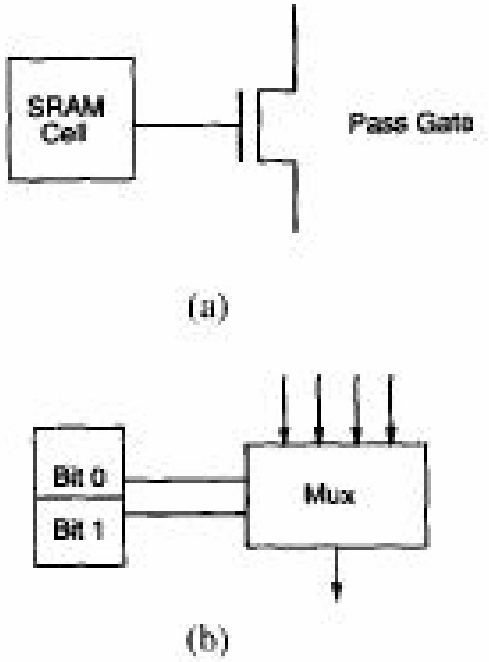
RAM dinamic

DRAM

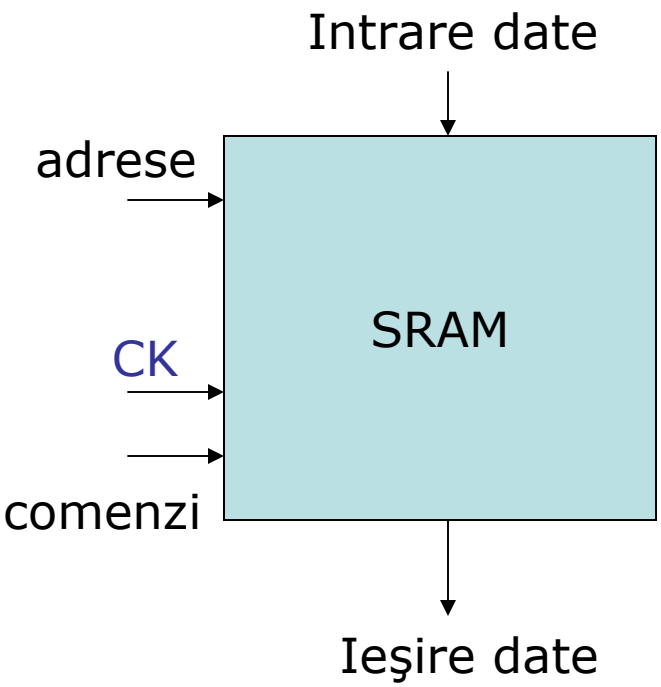
Conexiuni programabile cu SRAM

- tranzistorul de trecere: deschis cu 1 logic pe poartă

- MUX: memorarea celor 2 biţi de selecţie



Proiectarea memoriei SRAM în Verilog

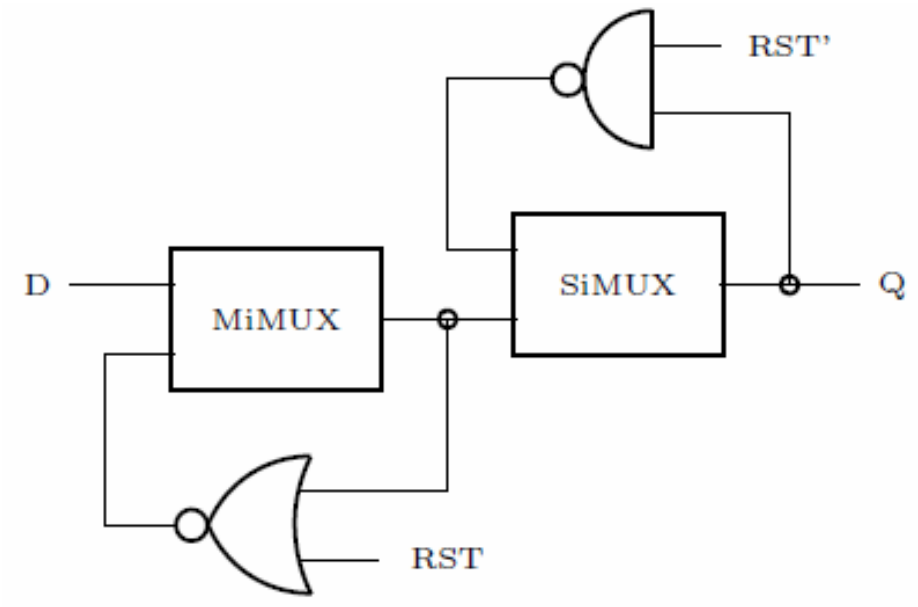


- Trebuie să alegem tipul memoriei, dimensiunea şi tipul comenzilor
- SRAMul este în esență o **matrice de date**
- În Verilog NU există matrici
- Descrierea în Verilog este comportamentală
- Se pot include:
  - Inițializări
  - Fişiere de date

Variante de ram şi de comenzi

- sincron/asincron
- comenzi:
  - we
  - read
  - oe
- prioritatea comenzilor (ordinea de execuţie)

Tema 7



- Desenaţi schema cu tranzistoare
- explicaţi funcţionarea circuitului

Aplicaţii

- bistabil D cu inversor tristate
- numărătorul