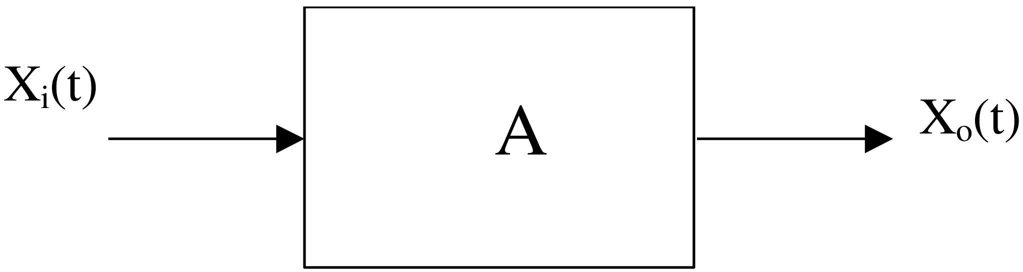
Chapter 3

Amplifier stages

3.1. Introduction

3.1. Introduction



$$X_o(t) = AX_i(t-\tau) \qquad P_o > P_i$$

(for linear amplifiers)

3.1.1. Parameters

3.1.1. Parameters:

$$Z_i = \frac{v_I}{i_I}$$

$$A_i = \frac{i_O}{i_I}$$

$$A_z = \frac{v_O}{i_I}$$

$$Z_o = \frac{v_O}{i_O}$$

$$A_Y = \frac{i_O}{v_I}$$

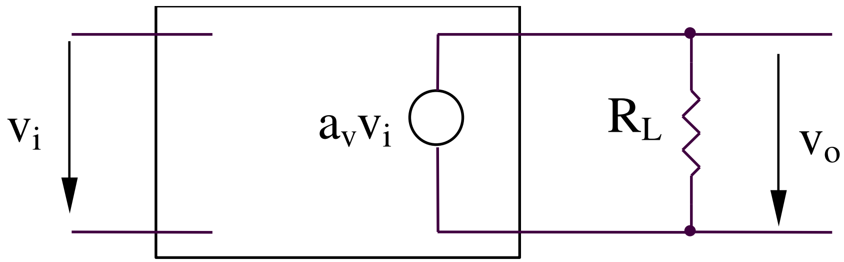
$$A_v = \frac{v_O}{v_I}$$

$$A_p = \frac{P_O}{P_I}$$

3.1.2. Ideal amplifiers

3.1.2. Ideal amplifiers

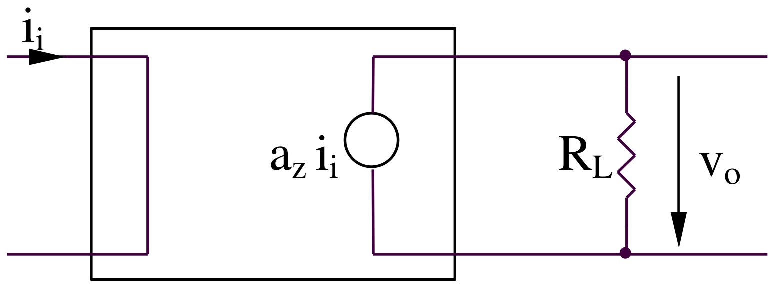
Voltage amplifier



$$v_O = a_v v_I \qquad i_I = 0; P_i = 0$$

$$R_i \to \infty; R_o = 0$$

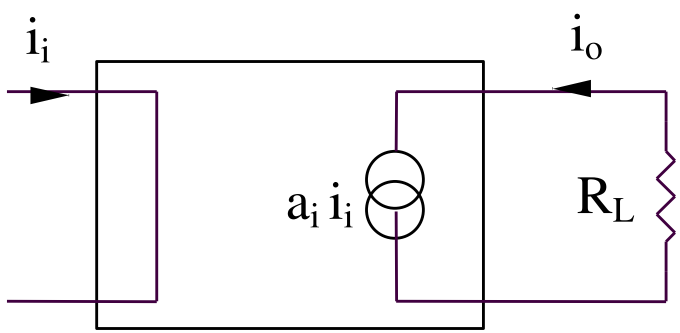
Transimpedance amplifier



$$v_O = a_z i_I \qquad v_I = 0; P_i = 0$$

$$R_i = 0; R_o = 0$$

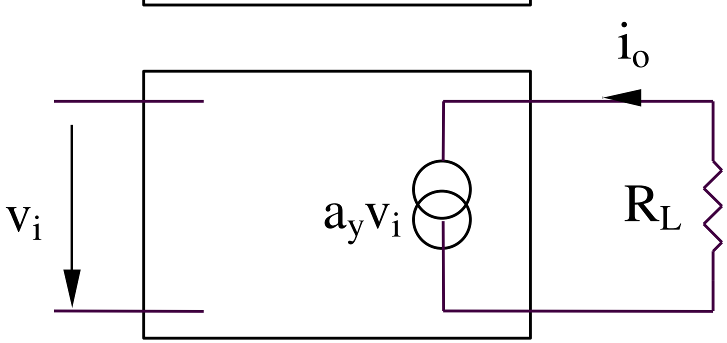
Current amplifier



$$i_O = a_i i_I \qquad v_I = 0; P_i = 0$$

$$R_i = 0; R_o \to \infty$$

Transadmitance amplifier



$$i_O = a_y v_I \qquad i_I = 0; P_i = 0$$

$$R_i \to \infty; R_o \to \infty$$

3.2. The coupling of amplifiers

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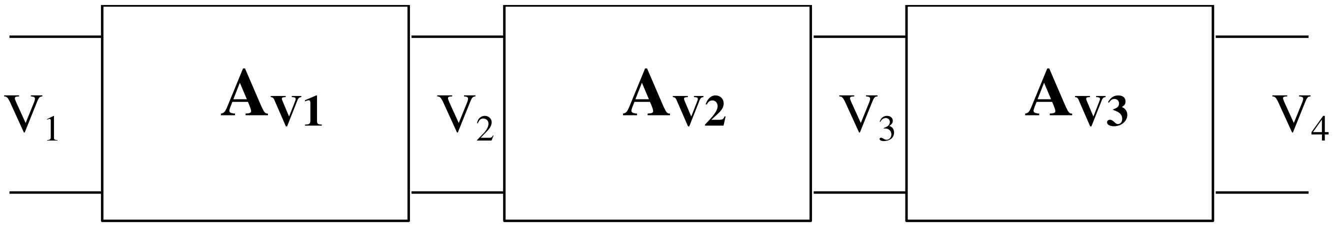


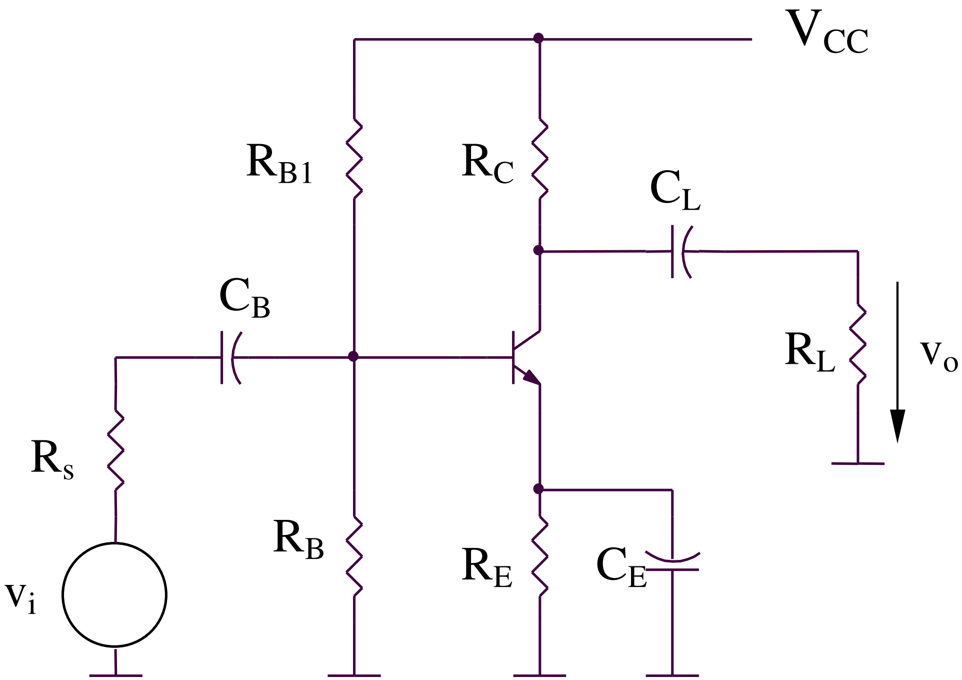
$$A_V = \frac{V_4}{V_1} = A_{V1} A_{V2} A_{V3}$$

$$A_V(dB) = A_{V1}(dB) + A_{V2}(dB) + A_{V3}(dB)$$

3.3. Amplifier stage with one transistor

3.3.1. Common-emitter stage

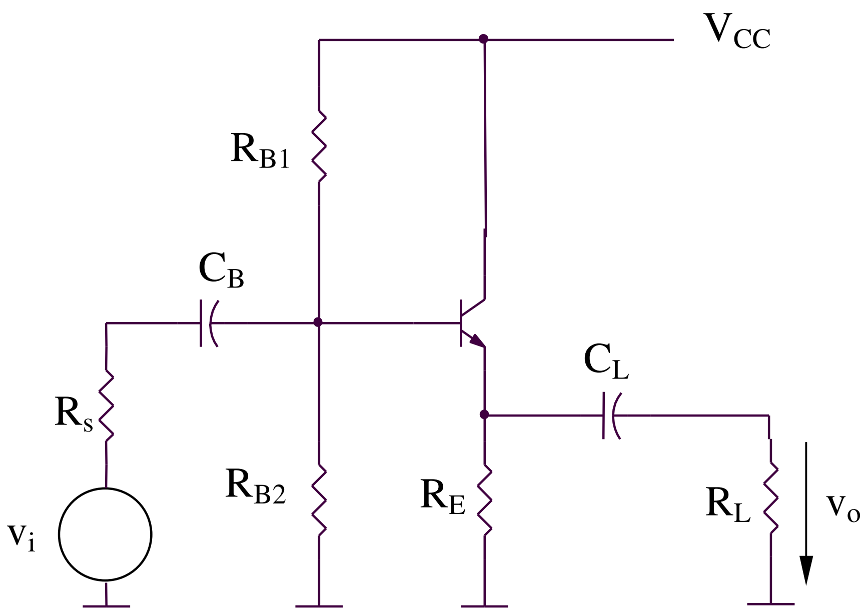
3.3.1. Common-emitter stage



$$A_V = -g_m \left(R_C \,//\, R_L \right)$$
$$R_i = r_\pi \,//\, R_{B1} \,//\, R_{B2}$$
$$R_o = R_L \,//\, R_C \,//\, r_o$$

3.3.2. Common collector stage

3.3.2. Common collector stage



$$A_V = \frac{(\beta+1)(R_E \mathbin{//} R_L)}{r_\pi + (\beta+1)(R_E \mathbin{//} R_L)}$$

$$R_i = R_{B1} \mathbin{//} R_{B2} \mathbin{//} [r_\pi + (\beta+1)(R_E \mathbin{//} R_L)]$$

$$R_o = R_E \mathbin{//} R_L \mathbin{//} 1/g_m$$

3.3.3. Common-base stage

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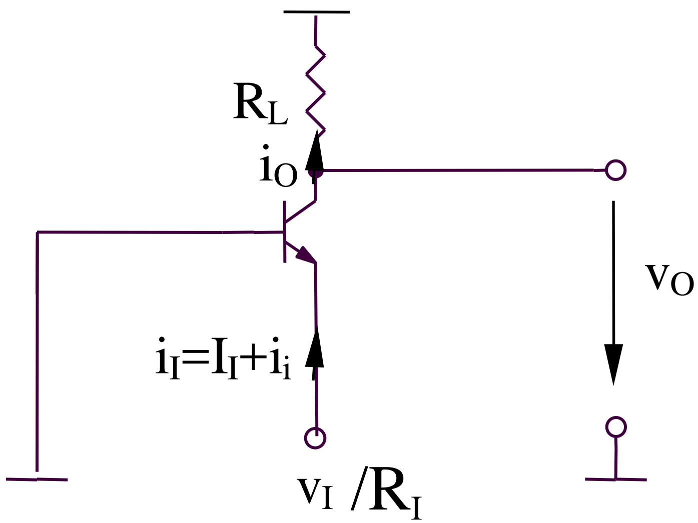

$$A_i = \frac{i_O}{i_I} \cong 1$$

$$A_v = \frac{v_o}{v_i} = g_m R_L$$

$$R_i = \frac{1}{g_m}$$

$$R_o = R_L \,//\, r_o\left(1 + \frac{\beta R_I}{r_\pi + R_I}\right)$$

3.3.4. Distributed load stage

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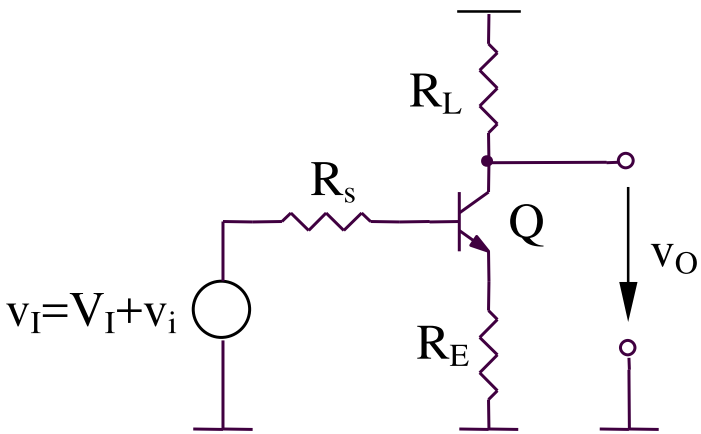


$$A_v = \frac{v_O}{v_I} = \frac{v_O}{i_C}\frac{i_C}{i_B}\frac{i_B}{v_I}$$

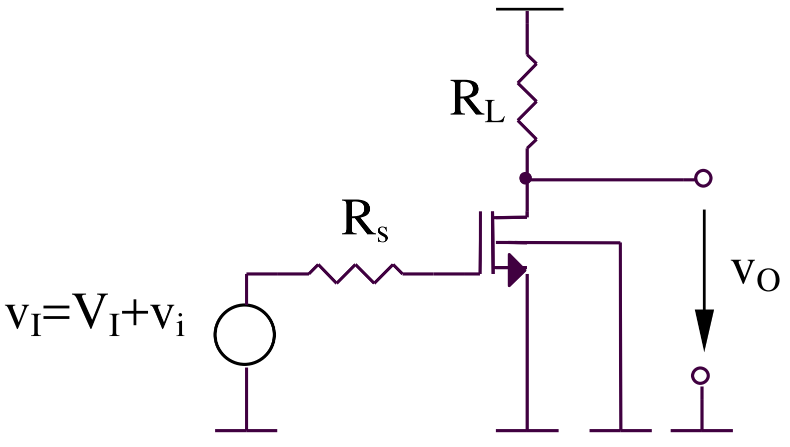
$$A_v = -\frac{\beta R_L}{R_s + r_\pi + (\beta + 1)R_E}$$

$$R_i = R_s + r_\pi + (\beta + 1)R_E$$

$$R_o \cong R_L$$

3.3.5. Common source stage

3.3.5. Common source stage



$$A_v = \frac{v_O}{v_I} = \frac{-g_m v_{GS}(R_L // r_{ds})}{v_{GS}}$$

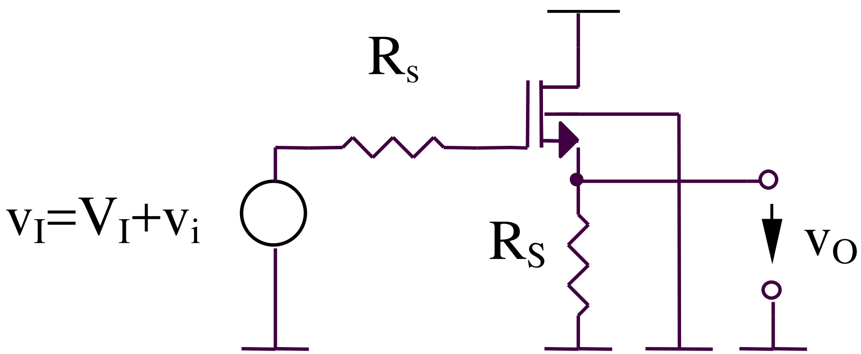
$$A_v = -g_m\left(R_L // r_{ds}\right)$$

$$R_i = \infty$$

$$R_o = R_L // r_{ds}$$

3.3.6. Common drain stage

3.3.6. Common drain stage



$$A_v = \frac{v_O}{v_I} = \frac{g_m v_{GS} R_S}{v_{GS} + g_m v_{GS} R_S}$$

$$A_v = \frac{g_m R_S}{1 + g_m R_S} \cong 1$$

$$R_i = \infty$$

$$R_o = \frac{1}{g_m} // R_S$$

3.3.7. Common gate stage

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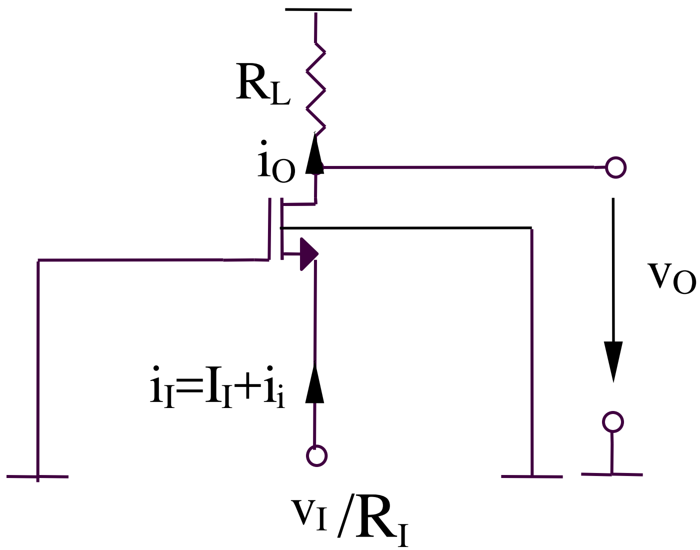

$$A_v = \frac{v_O}{v_I} = \frac{-g_m v_{GS} R_L}{-v_{GS}}$$

$$A_v = g_m R_L$$

$$R_i = \frac{1}{g_m}$$

$$R_o = R_L \, // \, r_{ds}\left(1 + g_m R_I\right)$$

3.3.8. Distributed load stage

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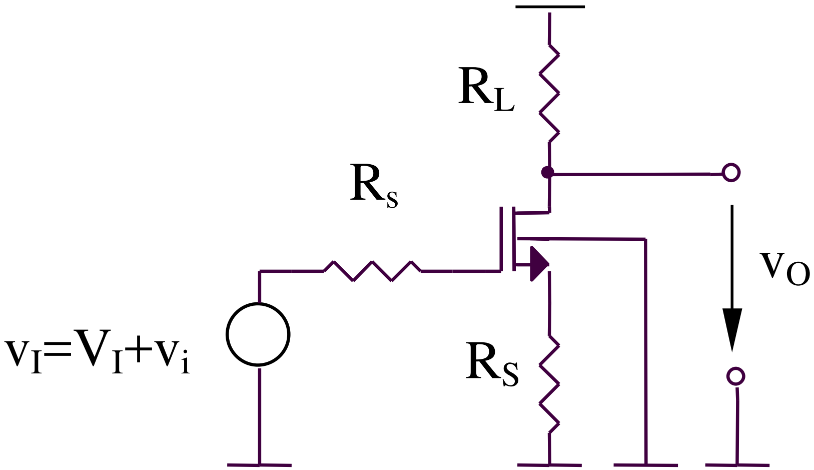


$$A_v = \frac{v_O}{v_I} = \frac{-g_m v_{GS} R_L}{v_{GS} + g_m v_{GS} R_S}$$

$$A_v = -\frac{g_m R_L}{1 + g_m R_S}$$

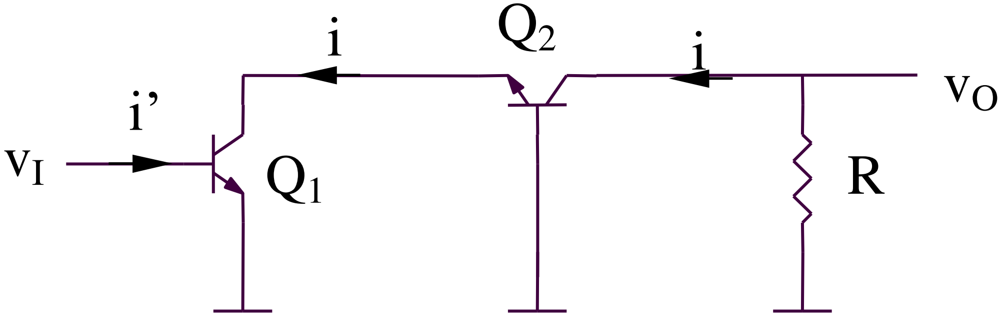
$$R_i = \infty$$

$$R_o \cong R_L$$

3.4. Amplifier stages with two transistors

3.4.1. Cascode stage

3.4.1. Cascode stage



$$A_V = \frac{v_O}{v_I} = \frac{v_O}{i}\frac{i}{i'}\frac{i'}{v_I} = -R\beta\frac{1}{r_{\pi 1}} = -g_{m1}R$$

3.5. Bipolar differential amplifier

3.5. Bipolar differential amplifier

- part of many analog integrated circuits
- the two transistors must have characteristics as identical as possible
- the resistance R_{EE} could be replaced with a current source having a much greater output resistance

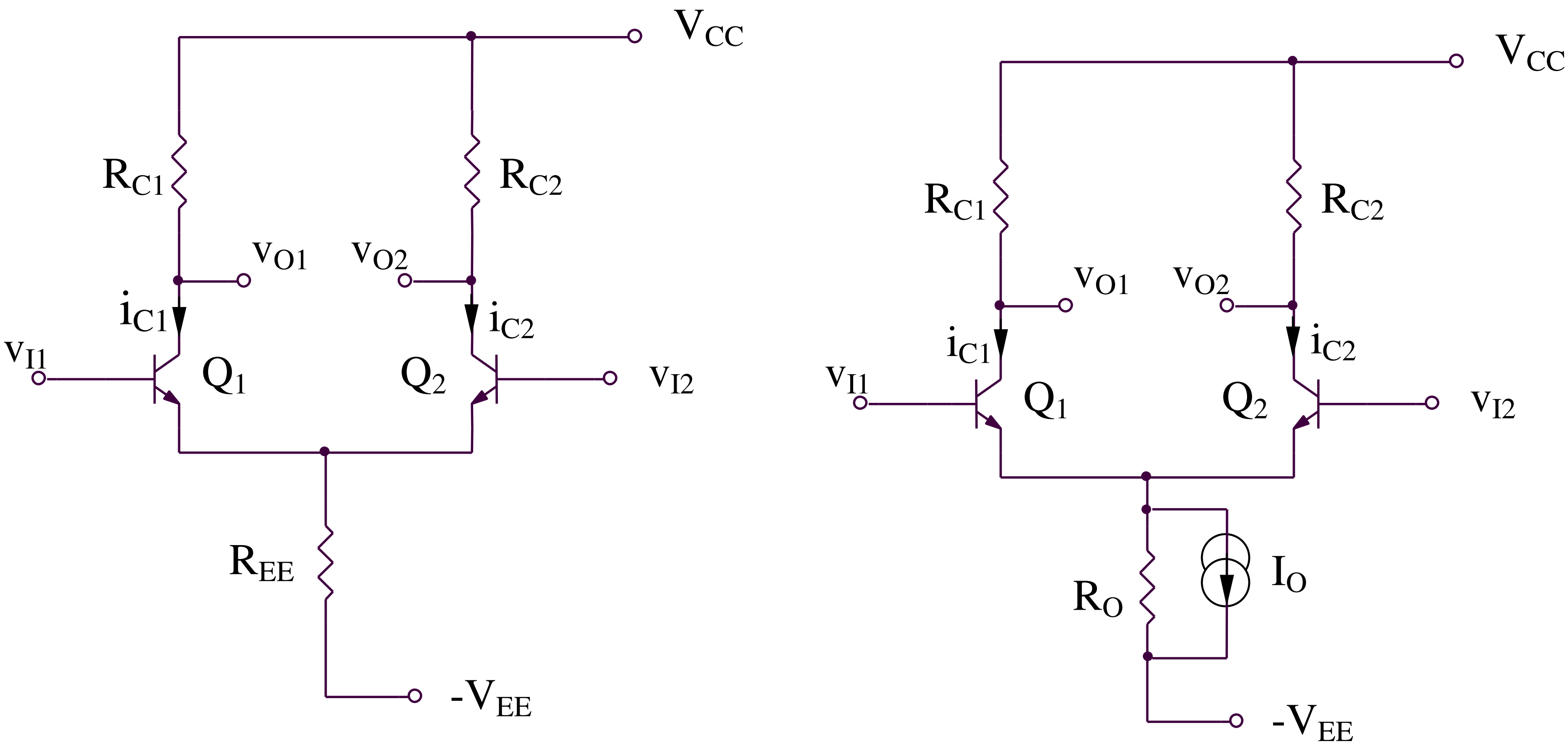
The output could be taken:

- symmetrical:

$$R_{C1} = R_{C2} \qquad v_O = v_{O1} - v_{O2} = A(v_{I1} - v_{I2})$$

- asymmetrical:

$$v_O = v_{O1} \;\; ou \;\; v_{O2} = \pm A(v_{I1} - v_{I2})$$



(a) (b)

The differential stage has properties adapted to integration

- DC operation
- requirements for matched devices
- requirement for the same temperature of the transistors

3.5.1. Large signal analysis

3.5.1. Large signal analysis

$$I_O = i_{E1} + i_{E2}$$
$$I_O \cong i_{C1} + i_{C2}$$

$$I_O = I_S\left(e^{\frac{v_{BE1}}{V_{th}}} + e^{\frac{v_{BE2}}{V_{th}}}\right)$$

$$I_O = I_S e^{\frac{v_{BE1}}{V_{th}}}\left(1 + e^{\frac{v_{BE2}-v_{BE1}}{V_{th}}}\right)$$

But:

$$i_{C1} = I_S e^{\frac{v_{BE1}}{V_{th}}}$$
$$v_{BE2} - v_{BE1} = v_{I2} - v_{I1}$$

It is possible to write the expressions of collector currents:

$$i_{C1} = \frac{I_O}{1 + e^{\frac{v_{I2}-v_{I1}}{V_{th}}}} = \frac{I_O}{2}\left(1 + th\frac{v_{I1} - v_{I2}}{2V_{th}}\right)$$

$$i_{C2} = \frac{I_O}{1 + e^{\frac{v_{I1}-v_{I2}}{V_{th}}}} = \frac{I_O}{2}\left(1 - th\frac{v_{I1} - v_{I2}}{2V_{th}}\right)$$

i_{C1} and i_{C2} could be developed in Taylor series:

$$\frac{i_{C1}(x)}{I_O} = \frac{1}{1+e^{-x}} = \frac{1}{2} + \frac{x}{4} - \frac{x^3}{48} + \dots$$

$$x = \frac{v_{I1} - v_{I2}}{V_{th}}$$

$$\frac{i_{C2}(x)}{I_O} = \frac{1}{1+e^{x}} = \frac{1}{2} - \frac{x}{4} + \frac{x^3}{48} - \dots$$

So, the tangent at characteristic $i_{C1}(x)/I_O$ has the following equation:

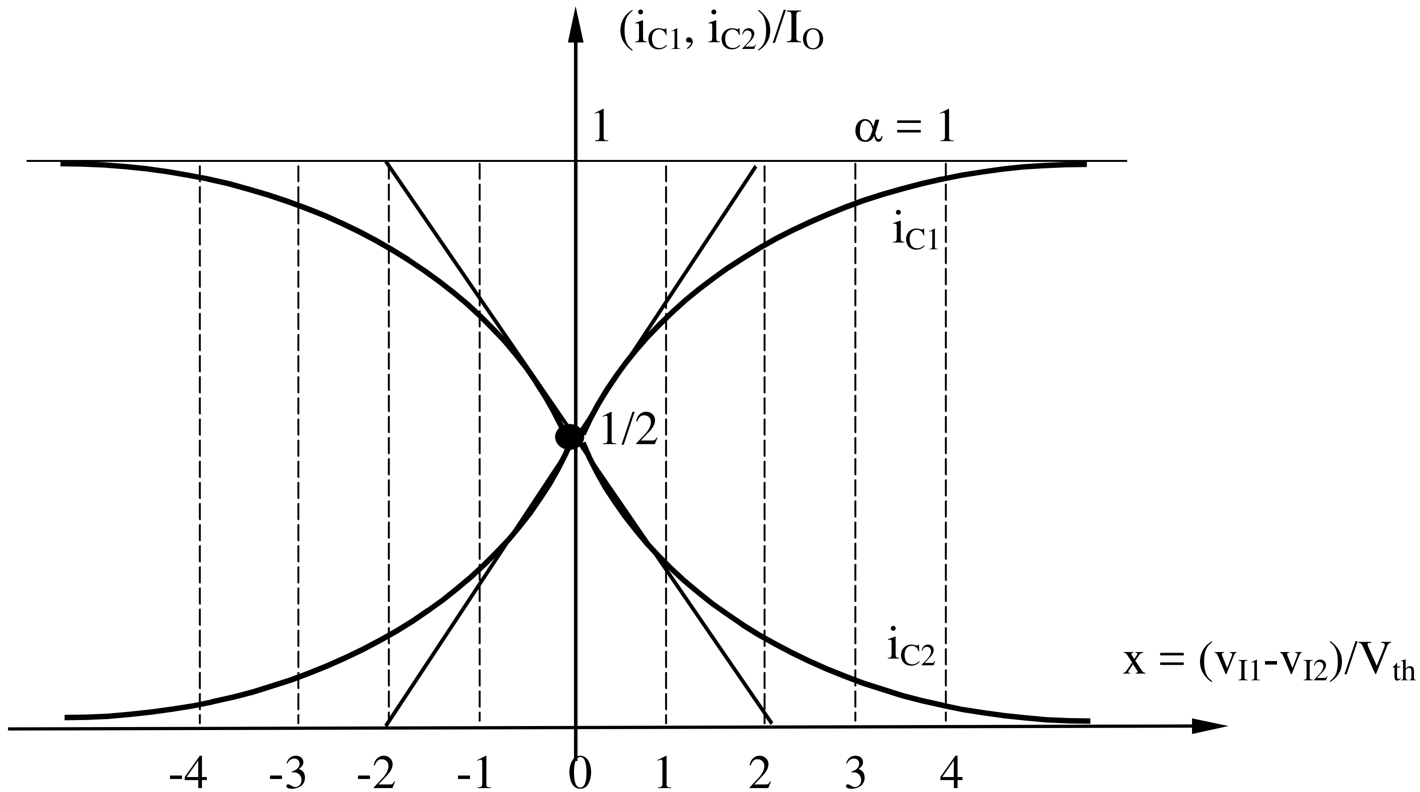
$$y = \frac{1}{2} + \frac{x}{4}$$

If:

$$y = 0 \Rightarrow x = -2 \Rightarrow v_{I1} - v_{I2} = -2V_{th} = -50mV$$

Remarks:

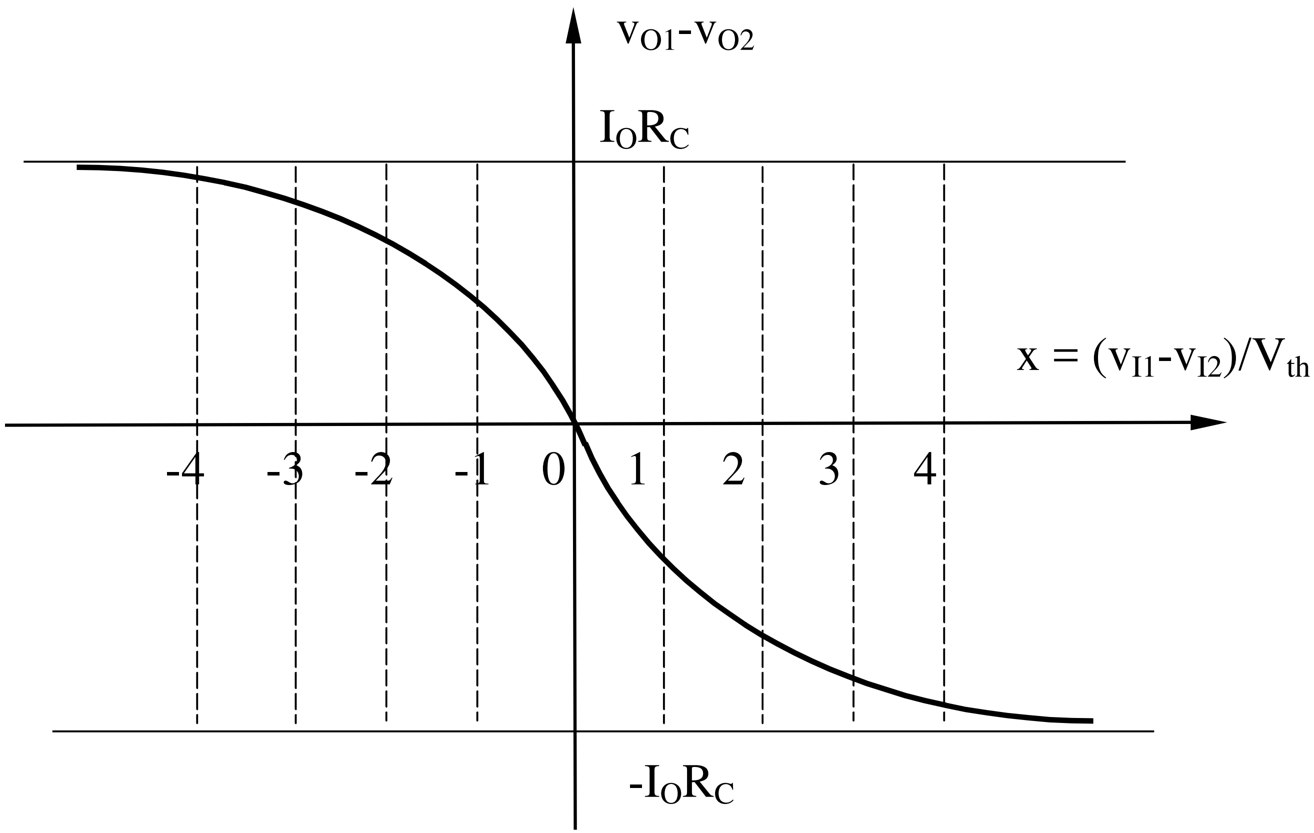
- for $v_{I1} = v_{I2}$ (or x = 0), $i_{C1} = i_{C2} = I_O/2$
- for a quasi-linear operation, the maximal amplitude of the input voltage must be less than $2V_{th}$ (or x =2), so about 50mV



Static characteristics $(i_{C1}, i_{C2})/I_O = f\,[(v_{I1}-v_{I2})/V_{th}]$
for the differential amplifier

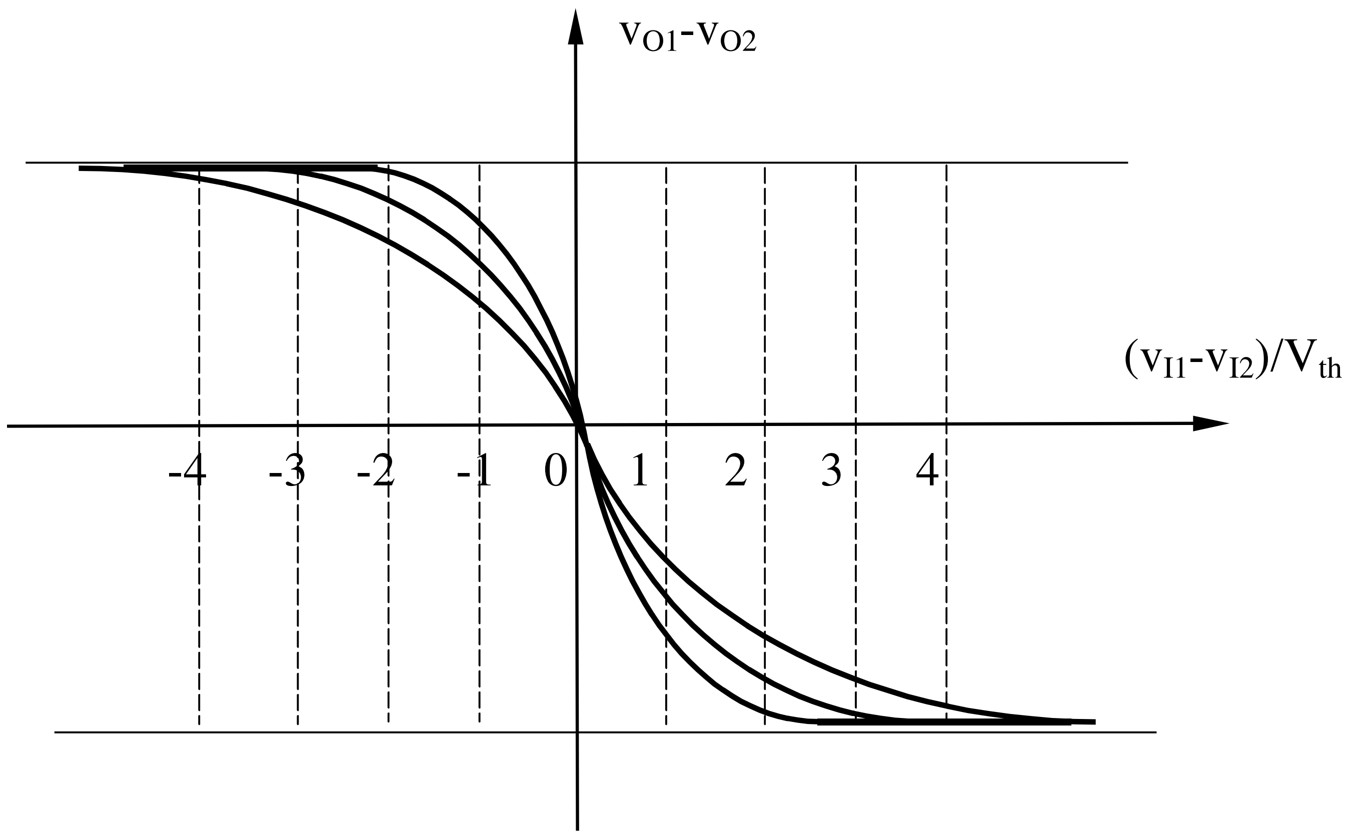
The output symmetrical voltage is:

$$v_O = v_{O1} - v_{O2} = (i_{C2} - i_{C1})R_C = \left(-\frac{x}{2} + \frac{x^3}{24} - \ldots\right) I_O R_C$$



Static characteristic $v_{O1}-v_{O2} = f\,[(v_{I1}-v_{I2})/V_{th}]$ for the differential amplifier

It is possible to increase the maximum range of the input voltage (for a linear operation of the circuit) by inserting two resistances in emitters (emitter degeneration).



3.5.2. Small signal analysis

3.5.2. Small signal analysis

There are: - differential mode (v_{id}, v_{od})
- common mode (v_{ic}, v_{oc})

$$v_{id} = \frac{v_{i1} - v_{i2}}{2}$$ differential input voltage

$$v_{od} = \frac{v_{o1} - v_{o2}}{2}$$ differential output voltage

$$v_{ic} = \frac{v_{i1} + v_{i2}}{2}$$ common-mode input voltage

$$v_{oc} = \frac{v_{o1} + v_{o2}}{2}$$ common-mode output voltage

$$\Rightarrow v_{i1} = v_{ic} + v_{id} \quad ; \quad v_{o1} = v_{oc} + v_{od}$$

$$v_{i2} = v_{ic} - v_{id} \quad ; \quad v_{o2} = v_{oc} - v_{od}$$

with the voltage gains:

$$A_{dd} = \left. \frac{v_{od}}{v_{id}} \right|_{v_{ic}=0}$$ differential gain

$$A_{cc} = \left. \frac{v_{oc}}{v_{ic}} \right|_{v_{id}=0}$$ gain in common-mode

it results:

$$v_{o1} = v_{od} + v_{oc} = A_{dd} v_{id} + A_{cc} v_{ic}$$

$$v_{o2} = v_{oc} - v_{od} = -A_{dd} v_{id} + A_{cc} v_{ic}$$

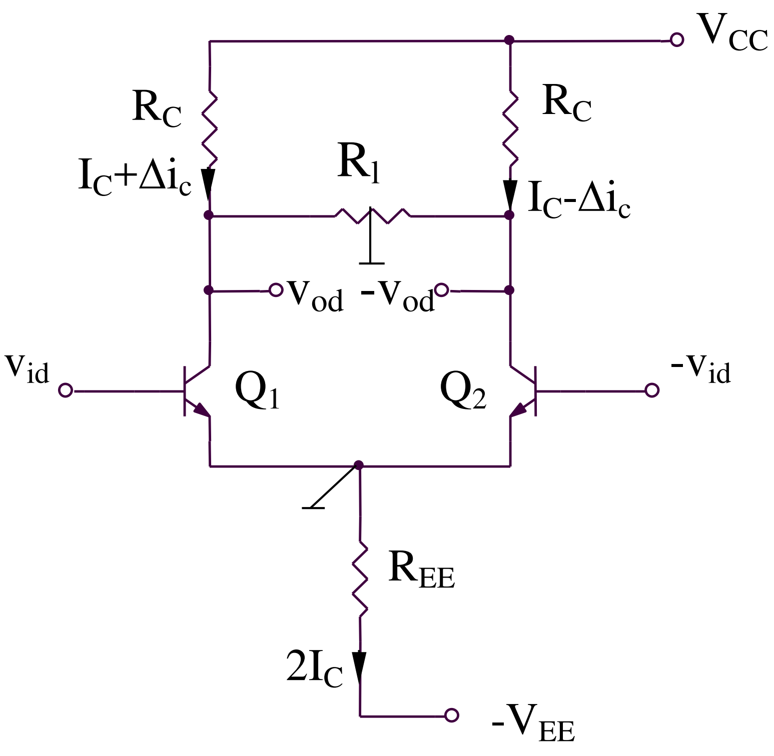
The common-mode rejection ratio is:

$$CMRR = \left| \frac{A_{dd}}{A_{cc}} \right|$$

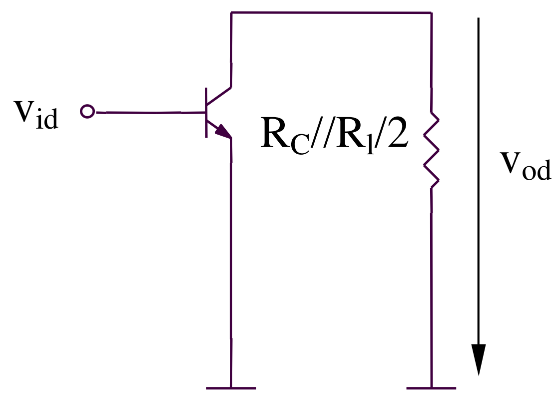
Determination of small signal gains: half-circuit method

Differential mode ($v_{id} \neq 0, v_{ic} = 0 \Rightarrow v_{i1} = v_{id}\ , v_{i2} = -\ v_{id}$)

An additional load resistance (R_l) has been introduced.



(a)



(b)

Voltage differential gain:

$$A_{dd} = \frac{v_{od}}{v_{id}} = -g_m\left(R_C \, // \, \frac{R_l}{2} \right)$$

- symmetrical output:

$$A = \frac{2v_{od}}{2v_{id}} = A_{dd}$$

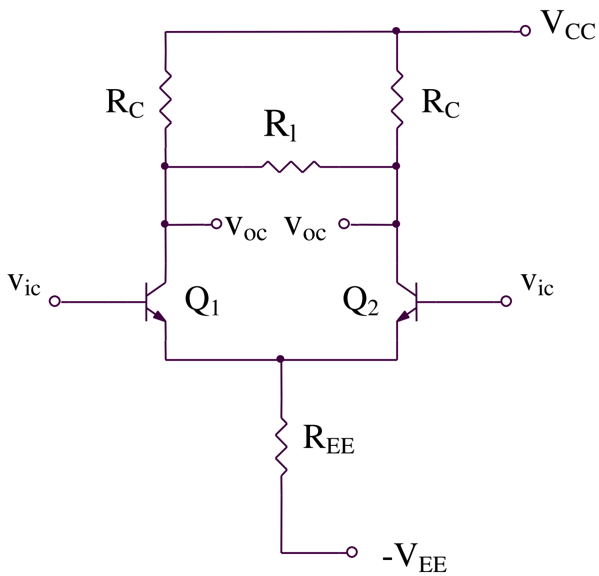
- asymmetrical output:

$$A = \frac{v_{od}}{2v_{id}} = \frac{A_{dd}}{2}$$

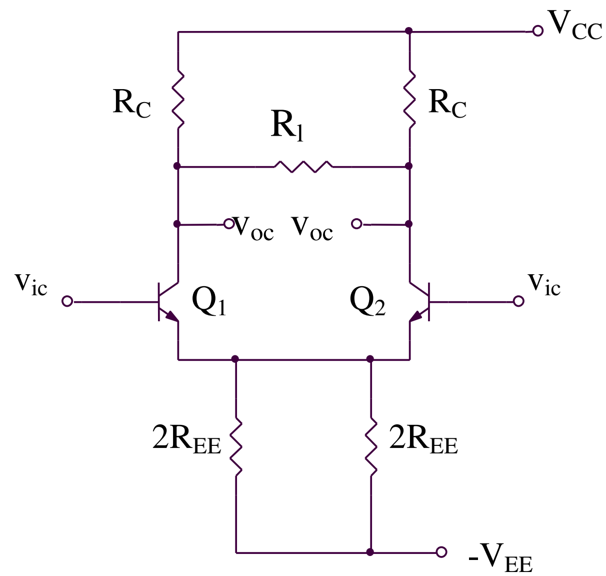
Differential input resistance:

$$R_{id} = 2r_{\pi}$$

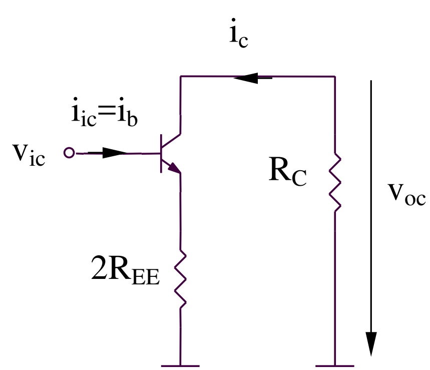
Common mode ($v_{ic} \neq 0, v_{id} = 0 \Rightarrow v_{i1} = v_{ic}\ , v_{i2} = - v_{ic}$)



(a)



(b)



(c)

Common-mode voltage gain:

$$A_{cc} = \frac{v_{oc}}{v_{ic}} = -\frac{\beta_0 R_C}{r_\pi + (\beta_0 + 1)2R_{EE}} \cong -\frac{R_C}{2R_{EE}}$$

Common-mode input resistance:

$$R_{ic} = \frac{v_{ic}}{i_{ic}} = r_\pi + (\beta_0 + 1)2R_{EE}$$

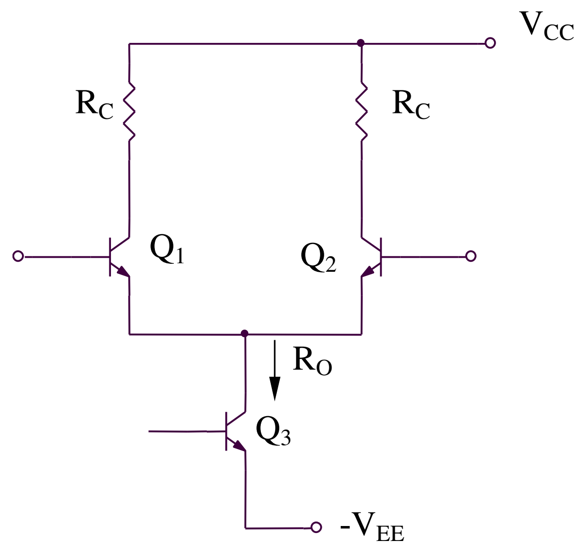
In consequence:

$$CMRR = \frac{I_{EE} R_{EE}}{V_{th}} \frac{\frac{R_l}{2} // R_C}{R_C}$$

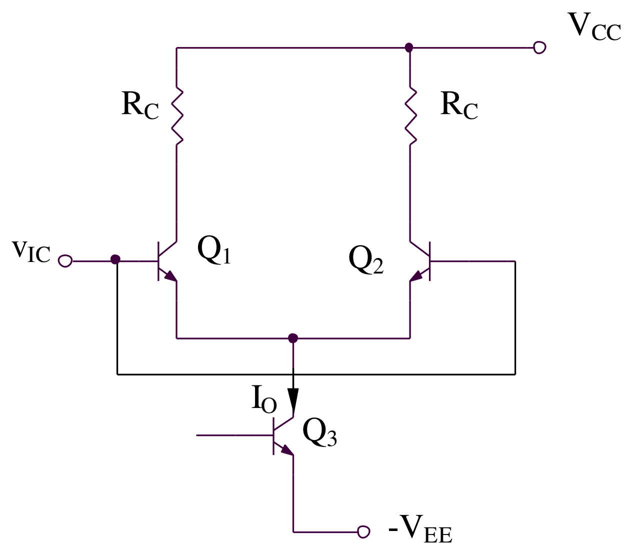
In order to increase CMRR, it is necessary to increase the voltage across R_{EE}, by replacing it with a current source:

$$A_{cc} = -\frac{R_C}{2R_O}$$

where R_O is the output resistance of Q_3.



Determination of common-mode input voltage range



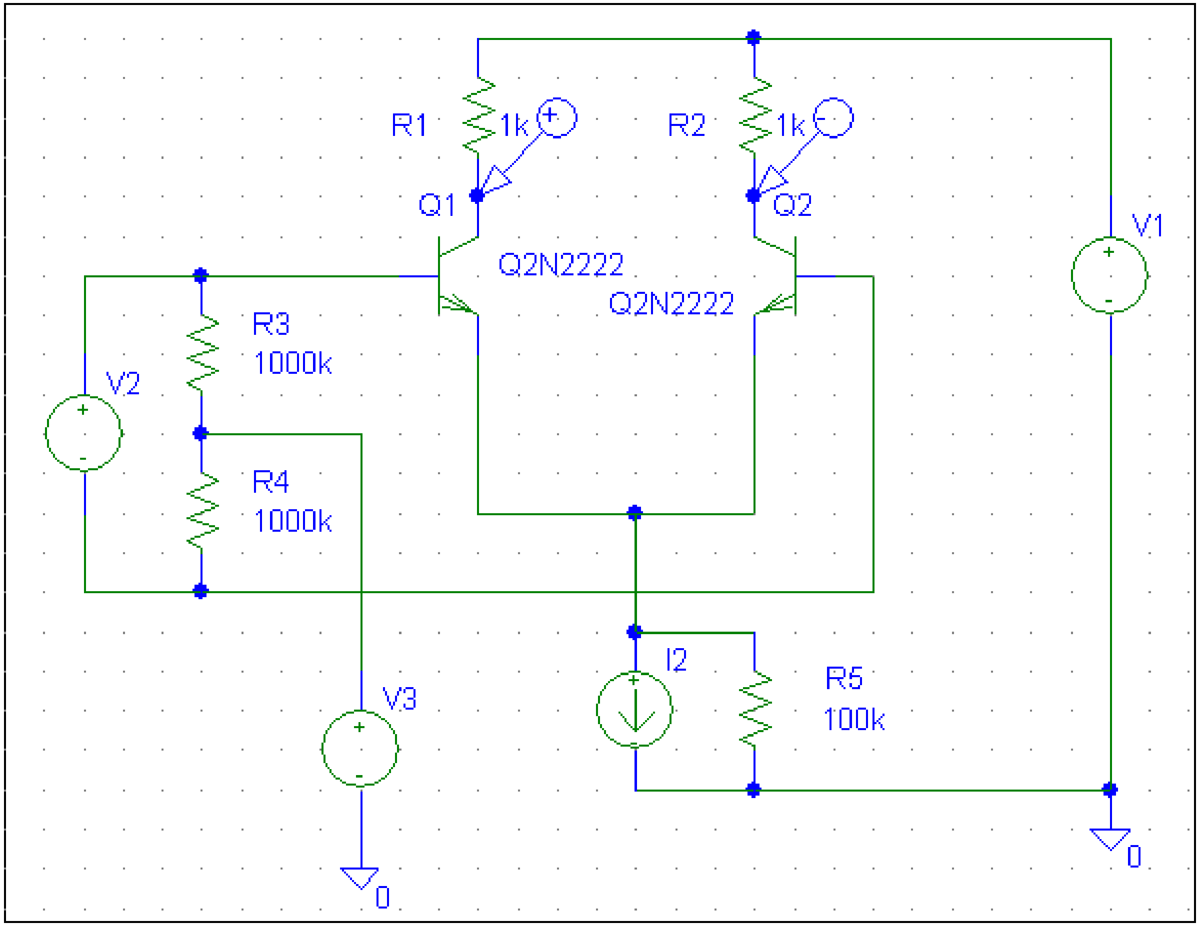
$$v_{IC}^{max} = V_{CC} - R_C \frac{I_O}{2} - V_{CE1sat} + V_{BE1}$$

$$v_{IC}^{min} = -V_{EE} + V_{CE3sat} + V_{BE1}$$

SIMULATIONS for bipolar differential amplifier
Differential-mode large signal analysis

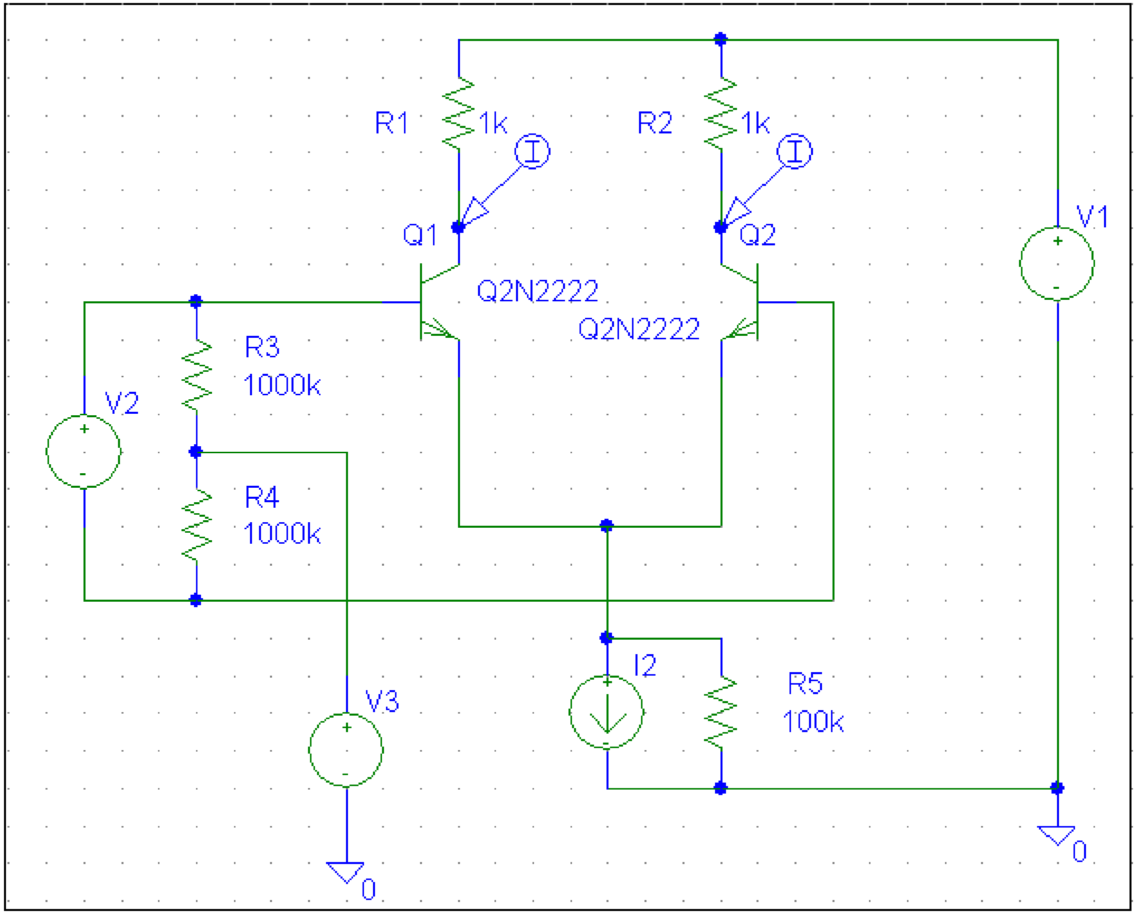
SIMULATIONS for bipolar differential amplifier
Differential-mode large signal analysis

SIM 3.1: V_O (V2)



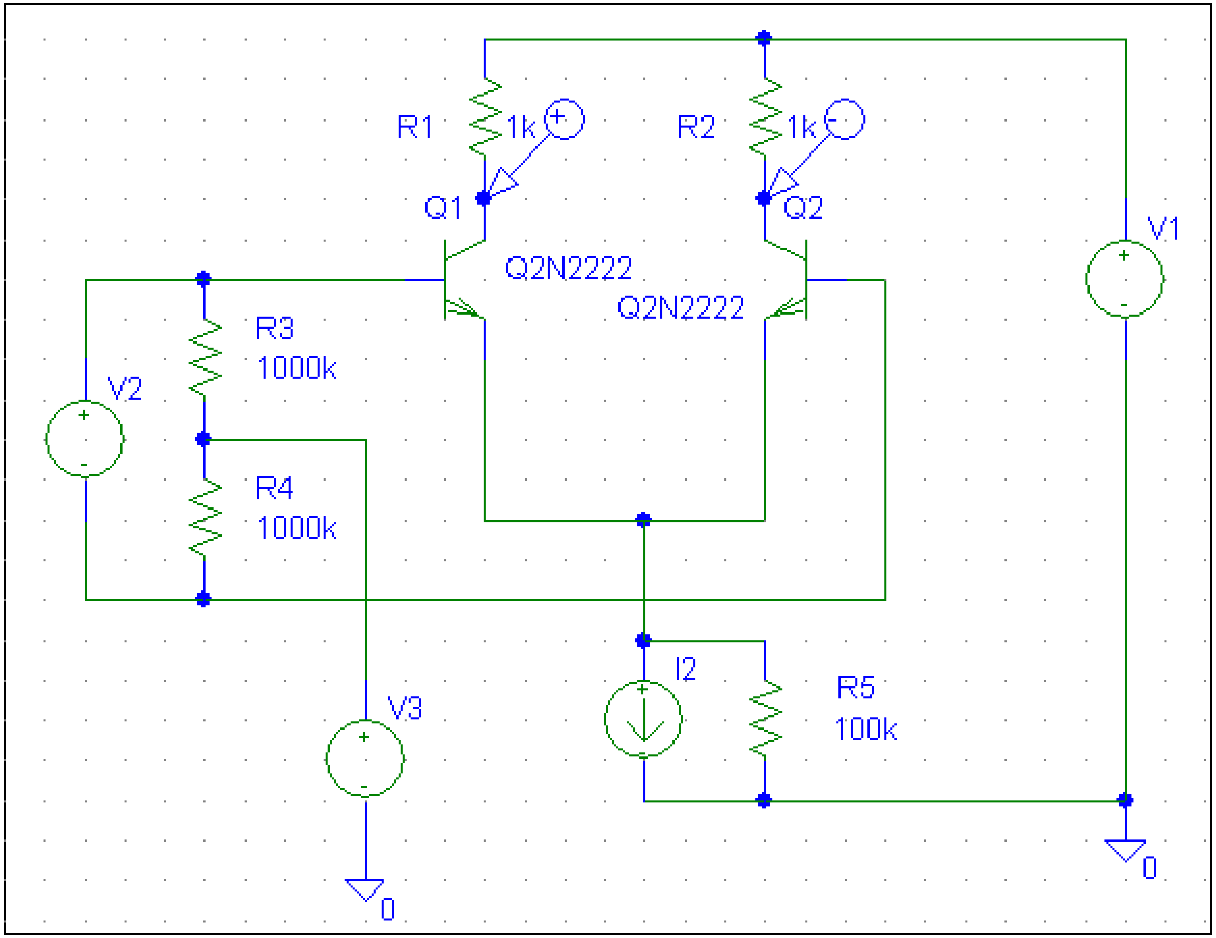
SIMULATIONS for bipolar differential amplifier
Differential-mode large signal analysis

SIM 3.2: i_{C1}, i_{C2} (V2)



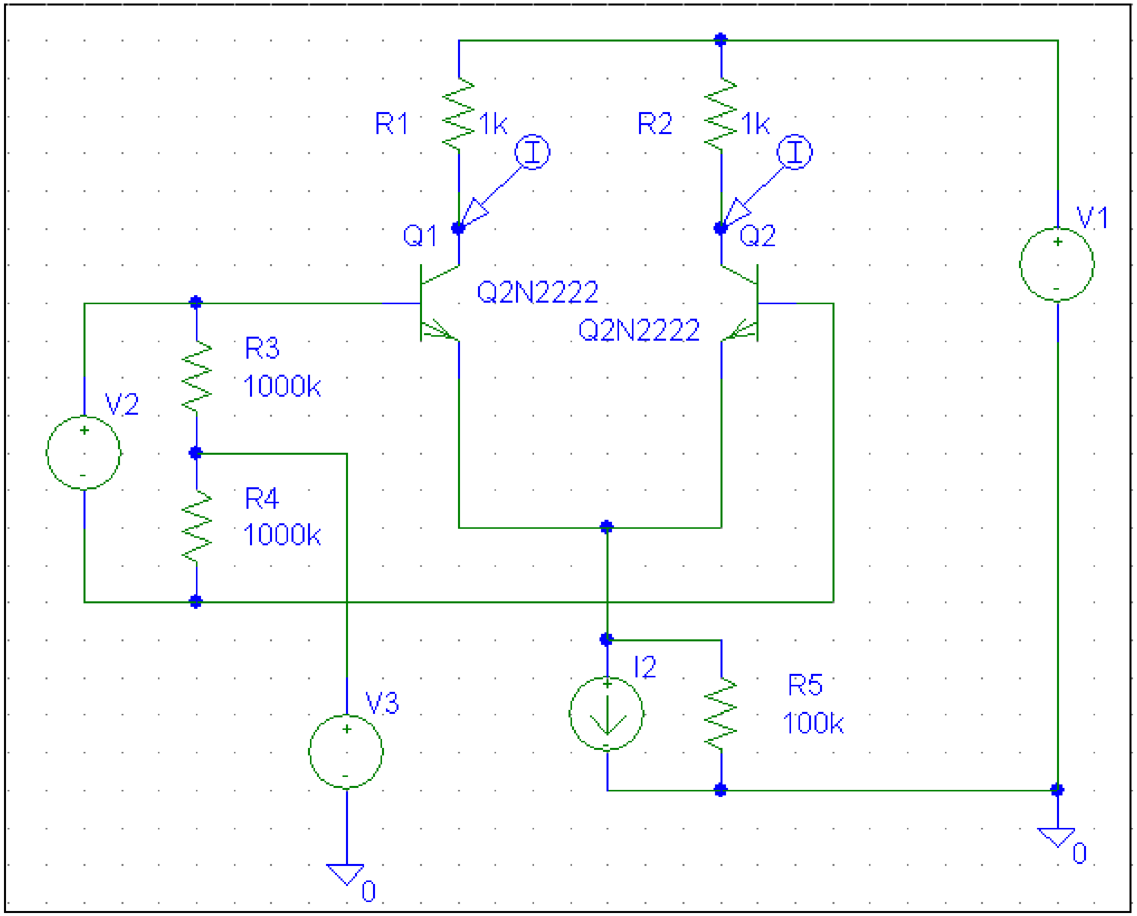
SIMULATIONS for bipolar differential amplifier
Differential-mode large signal analysis

SIM 3.3: V_O (V2), I2 - parameter



SIMULATIONS for bipolar differential amplifier
Differential-mode large signal analysis

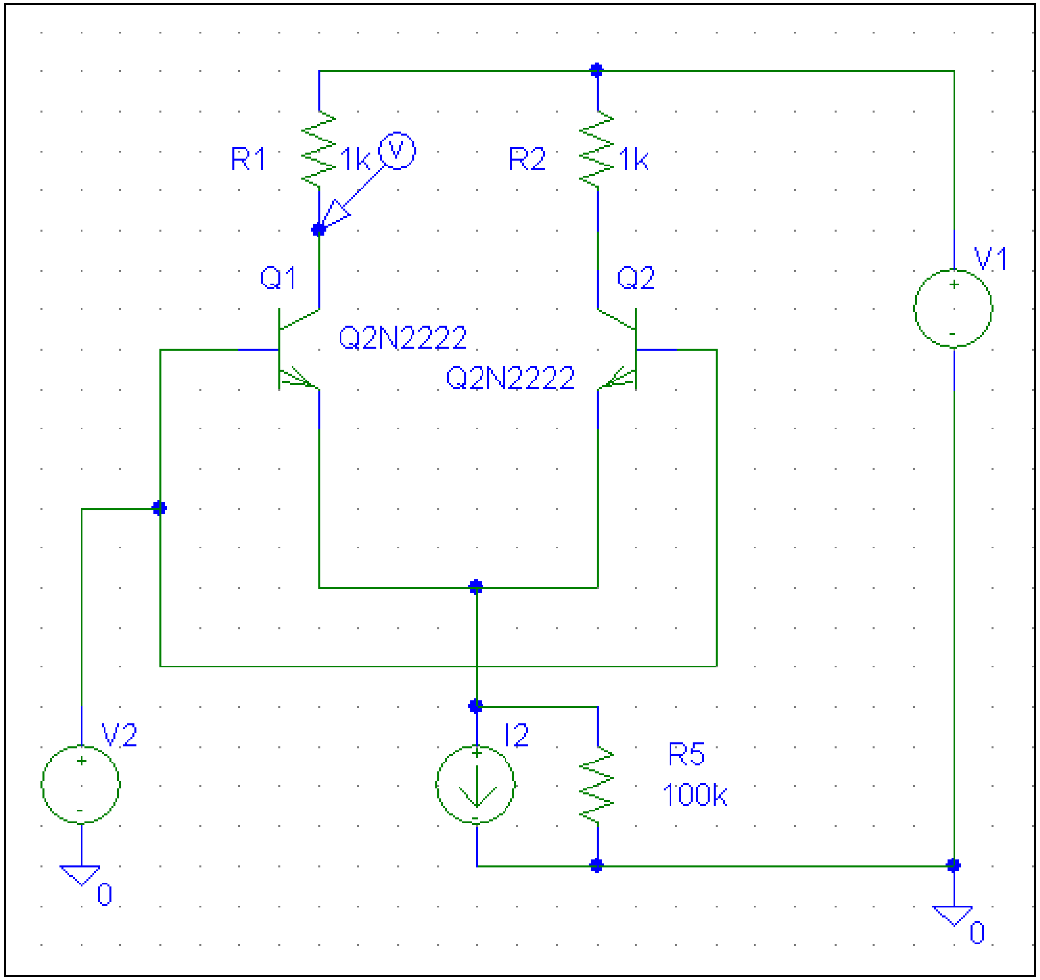
SIM 3.4: i_{C1}, i_{C2} (V2), I2 - parameter



SIMULATIONS for bipolar differential amplifier
Common-mode large signal analysis

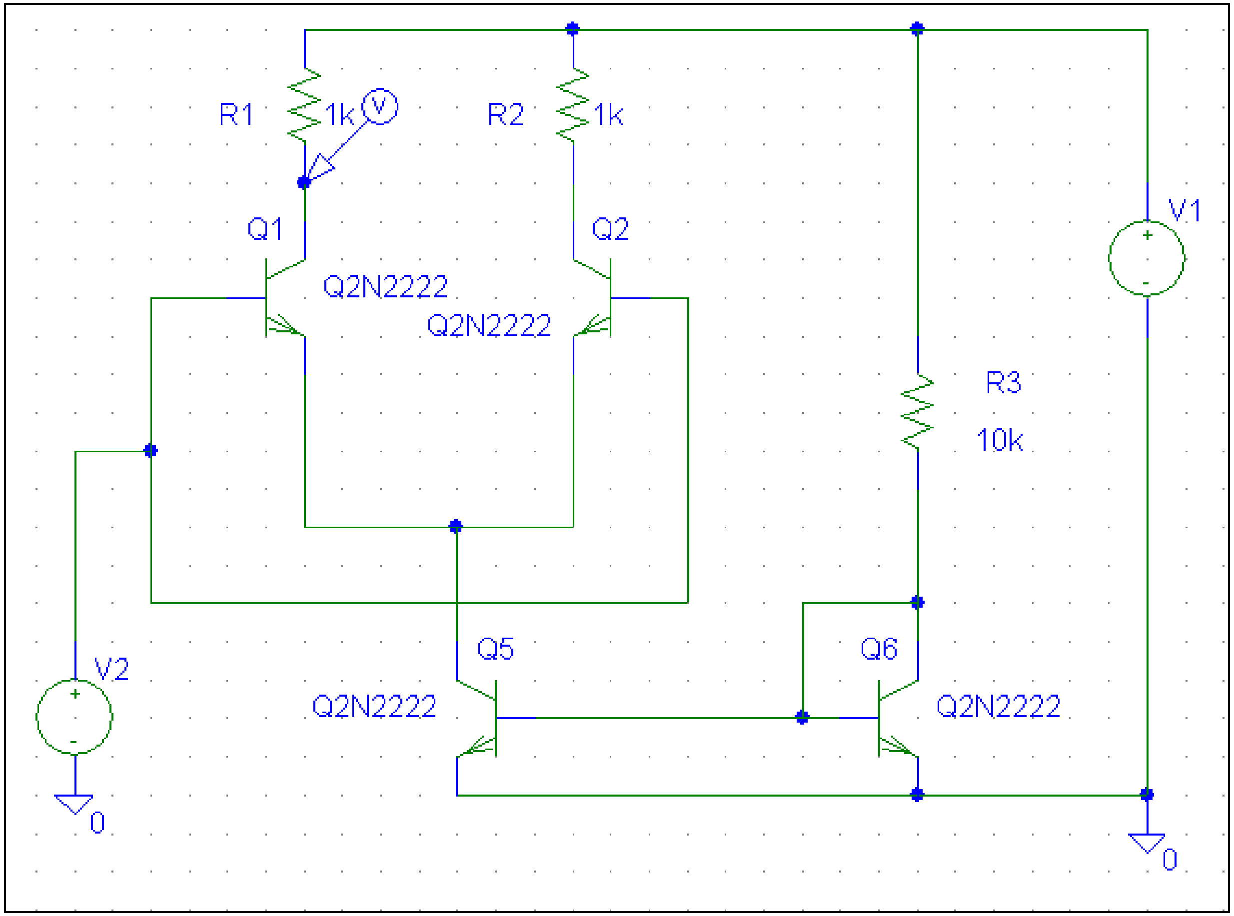
SIMULATIONS for bipolar differential amplifier
Common-mode large signal analysis

SIM 3.5: V_{C1} (V2)



SIMULATIONS for bipolar differential amplifier
Common-mode large signal analysis

SIM 3.6: V_{C1} (V2), V_{A5} - parameter



3.5.3. The input offset voltage

3.5.3. The input offset voltage

If the two transistors are not identical, it is necessary to apply a input voltage (named input offset voltage) in order to obtain a null output voltage.

$$v_{IO} = v_{BE1} - v_{BE2} = V_{th} \ln\left(\frac{i_{C1}}{i_{C2}} \frac{I_{S2}}{I_{S1}} \right)$$

Because:

$$i_{C1} R_{C1} = i_{C2} R_{C2}$$

it results:

$$v_{IO} = V_{th} \ln\left(\frac{R_{C2}}{R_{C1}} \frac{I_{S2}}{I_{S1}} \right)$$

Defining the parameters for describing the mismatch:

$$x = \frac{x_1 + x_2}{2} \qquad x_1 = x + \frac{\Delta x}{2}$$

$$\Delta x = x_1 - x_2 \qquad x_2 = x - \frac{\Delta x}{2}$$

it results:

$$v_{IO} = V_{th} \ln\left(\frac{R_C - \frac{\Delta R_C}{2}}{R_C + \frac{\Delta R_C}{2}} \frac{I_S - \frac{\Delta I_S}{2}}{I_S + \frac{\Delta I_S}{2}} \right) = V_{th} \ln\left(\frac{1 - \frac{\Delta R_C}{2R_C}}{1 + \frac{\Delta R_C}{2R_C}} \frac{1 - \frac{\Delta I_S}{2I_S}}{1 - \frac{\Delta I_S}{2I_S}} \right)$$

For:

$$\Delta R_C << R_C \ et \ \Delta I_S << I_S$$

$$x = \Delta R_C / 2R_C \ ou \ x = \Delta I_S / 2I_S$$

it is possible to write:

$$\frac{1-x}{1+x} \cong (1-x)(1-x) \cong 1 - 2x$$

So:

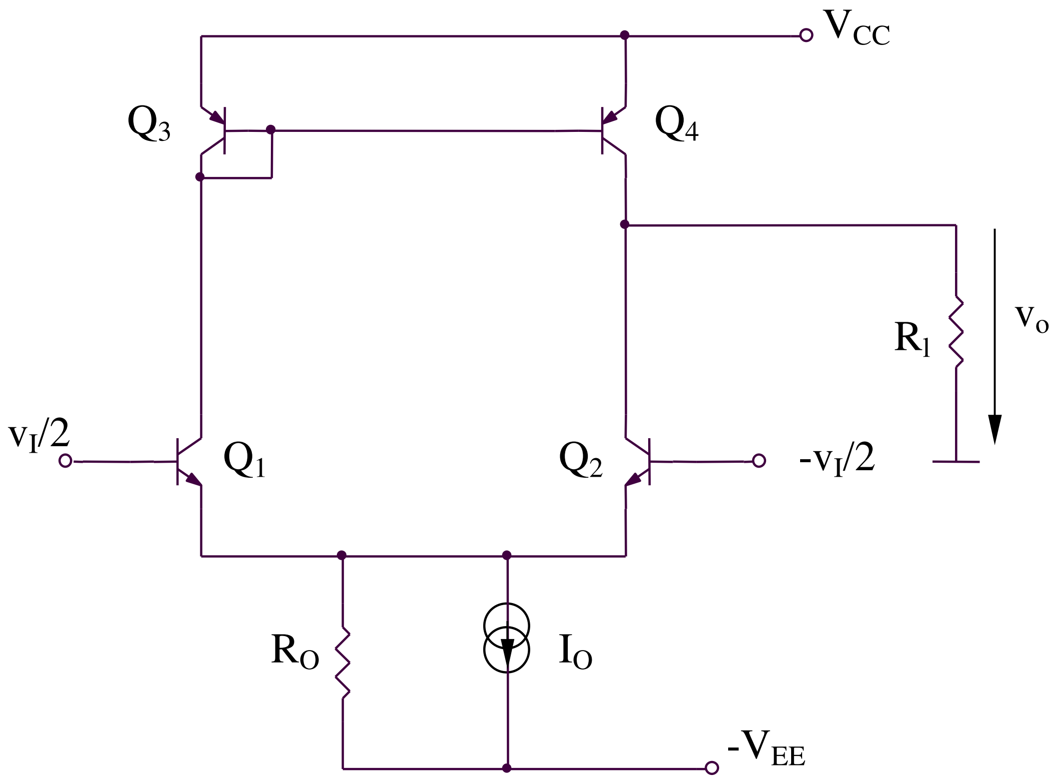
$$v_{IO} = V_{th} \ln\left[\left(1 - \frac{\Delta R_C}{R_C} \right)\left(1 - \frac{\Delta I_S}{I_S} \right) \right] = -V_{th}\left(\frac{\Delta R_C}{R_C} + \frac{\Delta I_S}{I_S} \right)$$

Usual case:

$$\frac{\Delta R_C}{R_C} = 0.01; \ \frac{\Delta I_S}{I_S} = 0.05 \Rightarrow v_{IO} = 1.5mV$$

3.5.4. Active load differential amplifier

3.5.4. Active load differential amplifier



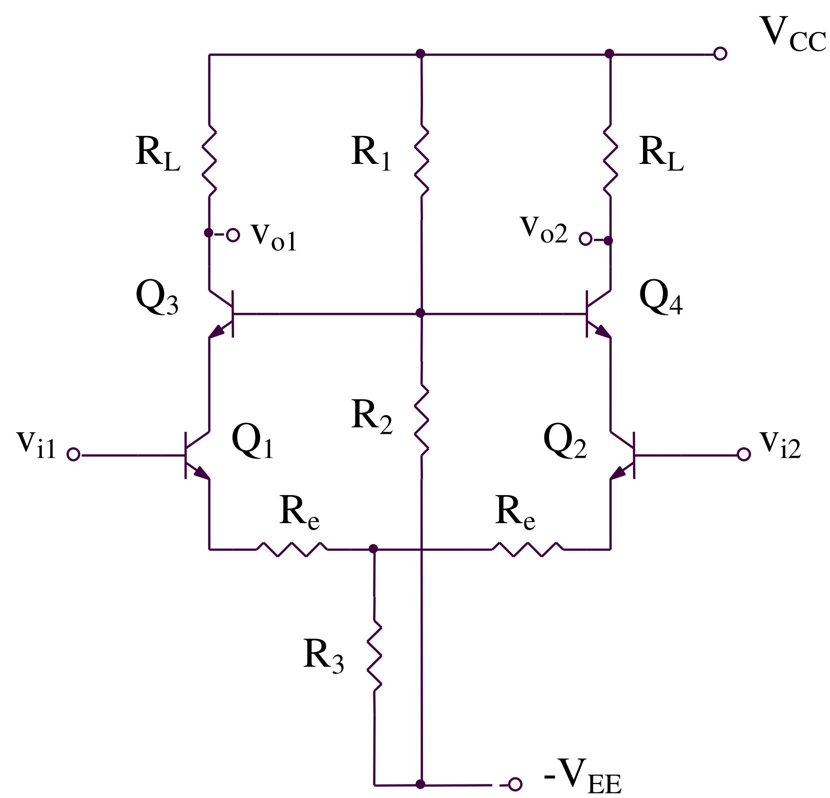
$$v_O = \left(g_{m1}\frac{v_I}{2} + g_{m2}\frac{v_I}{2} \right)\left(R_l // r_{o2} // r_{o4}\right) = g_{m1}v_I\left(R_l // r_{o2} // r_{o4}\right)$$

$$A_{dd} = g_{m1}\left(R_l // r_{o2} // r_{o4}\right)$$

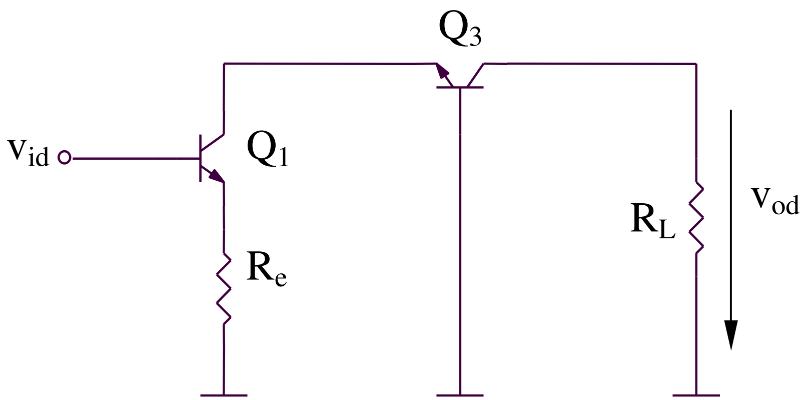
$$A_{dd}\Big|_{R_l \to \infty} = g_{m1}\left(r_{o2} // r_{o4}\right) = \frac{g_{m1}r_{o2}}{2} = \frac{I_{C1}}{2V_{th}}\frac{V_A}{I_{C1}} = \frac{V_A}{2V_{th}}$$

3.5.5. Cascode differential amplifier

3.5.5. Cascode differential amplifier



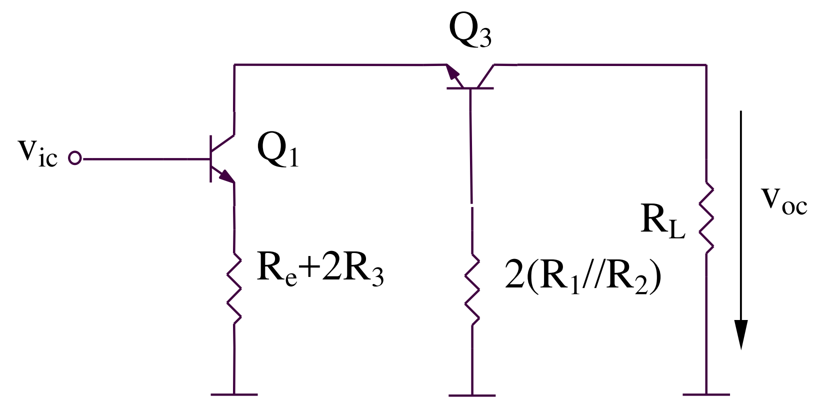
Differential mode



Differential mode half circuit

$$A_{dd} = -\frac{\beta R_L}{r_\pi + (\beta + 1)R_E}$$

Common mode

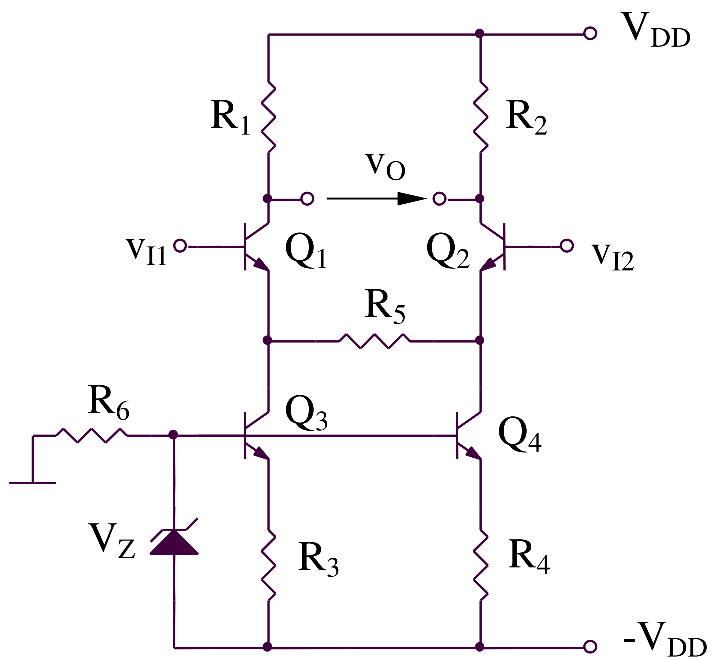


Common mode half circuit

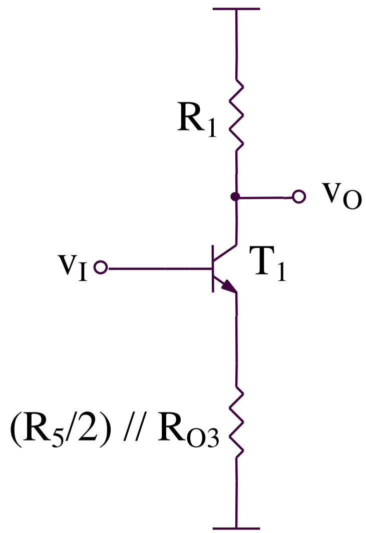
$$A_{cc} = -\frac{\beta R_L}{r_\pi + (\beta + 1)(R_E + 2R_3)}$$

3.5.6. Differential amplifier biased at a double current source

3.5.6. Differential amplifier biased at a double current source

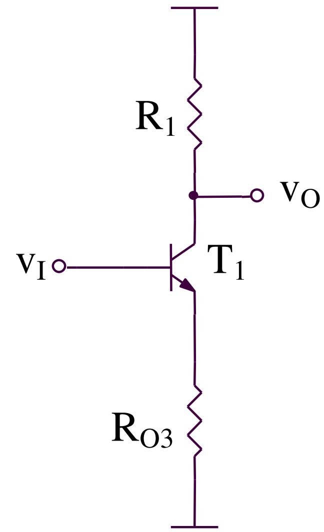


Differential mode



Differential mode half circuit

Common mode



Common mode half circuit

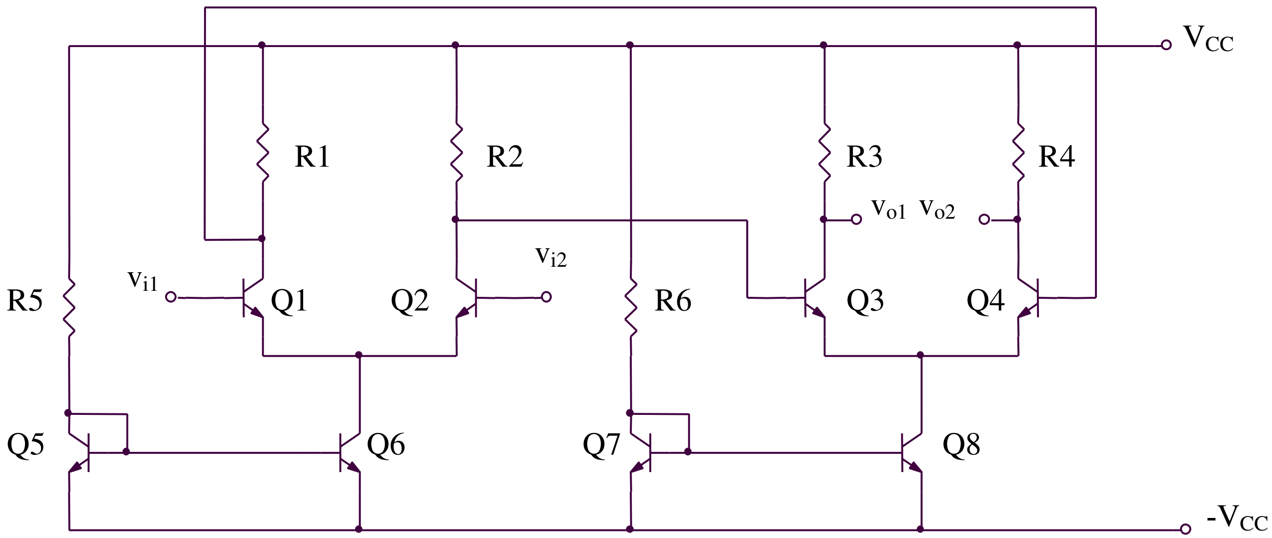
$$A_{dd} = -\frac{\beta R_1}{r_{\pi 1} + (\beta + 1)\left(\frac{R_5}{2} // R_{O3}\right)}$$

$$A_{cc} = -\frac{\beta R_1}{r_{\pi 1} + (\beta + 1) R_{O3}} \cong -\frac{R_1}{R_{O3}}$$

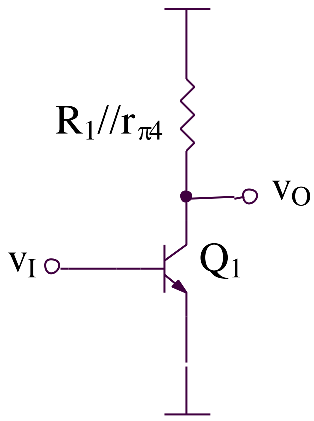
$$R_{O3} = r_{o3}\left(1 + \frac{\beta R_3}{r_{\pi 3} + R_3 + R_6 // r_Z}\right)$$

3.5.7. Structure using two differential amplifiers

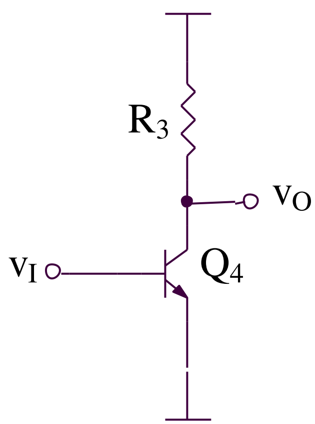
3.5.7. Structure using two differential amplifiers



Differential mode

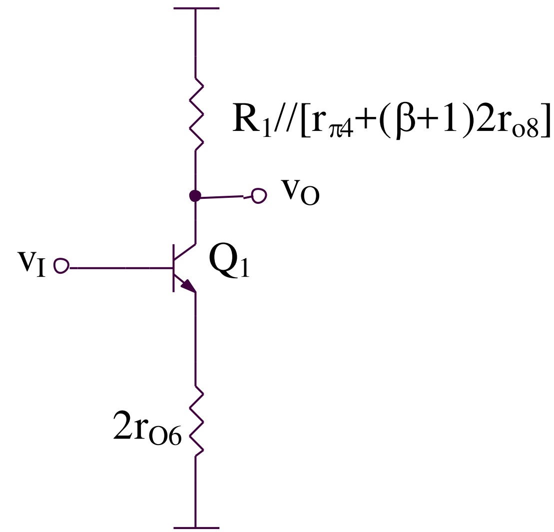


Differential mode half circuit (1)

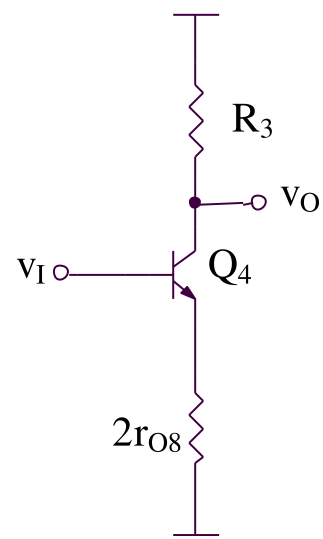


Differential mode half circuit (2)

Common mode



Common mode half circuit (1)



Common mode half circuit (2)

Differential mode gain (1)

$$A_{dd1} = -g_{m1}\left(R_1 \,//\, r_{\pi 4}\right)$$

Common mode gain (1)

$$A_{cc1} = -\beta \frac{R_1 \,//\left[r_{\pi 4} + (\beta + 1)2r_{o8}\right]}{r_{\pi 1} + (\beta + 1)2r_{o6}}$$

Differential mode gain (2)

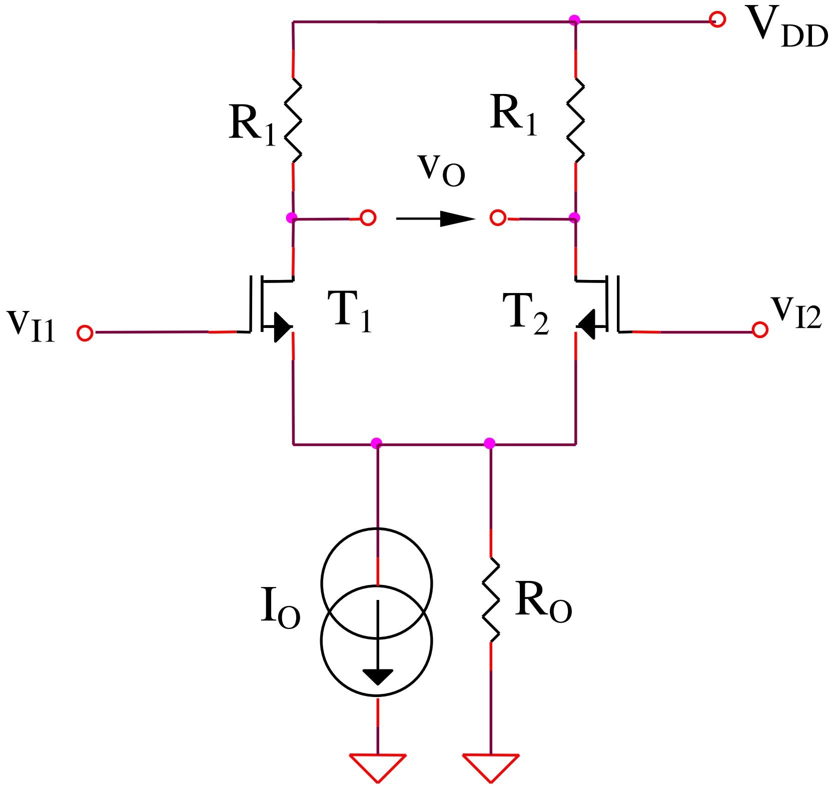
$$A_{dd2} = -g_{m4}R_3$$

Common mode gain (2)

$$A_{cc2} = -\beta \frac{R_3}{r_{\pi 1} + (\beta + 1)2r_{o8}}$$

3.6. MOS differential amplifiers

3.6. MOS differential amplifiers



3.6.1. Large signal analysis

3.6.1. Large signal analysis

$$v_{I1}-v_{I2}=v_{GS1}-v_{GS2}=\left(V_T+\sqrt{\frac{2i_{D1}}{K}}\right)-\left(V_T+\sqrt{\frac{2i_{D2}}{K}}\right)=\sqrt{\frac{2}{K}}\left(\sqrt{i_{D1}}-\sqrt{i_{D2}}\right)$$

$$i_{D1}+i_{D2}=I_O \qquad\qquad v_I=v_{I1}-v_{I2}$$

$$\Rightarrow i_{D1}^2-I_O i_{D1}+\frac{1}{4}\left(I_0-\frac{Kv_I^2}{2}\right)^2=0$$

So:

$$i_{D1}=\frac{I_O}{2}+\frac{I_O}{2}\sqrt{\frac{Kv_I^2}{I_O}-\frac{K^2v_I^4}{4I_O^2}} \qquad i_{D2}=\frac{I_O}{2}-\frac{I_O}{2}\sqrt{\frac{Kv_I^2}{I_O}-\frac{K^2v_I^4}{4I_O^2}}$$

For $v_I=\sqrt{\frac{2I_O}{K}}$ it results $i_{D1}=I_O, \quad i_{D2}=0$

The output voltage is

$$v_O=R_1\left(i_{D2}-i_{D1}\right)$$

$$v_O=-I_O R_1\sqrt{\frac{Kv_I^2}{I_O}-\frac{K^2v_I^4}{4I_O^2}}=-\frac{R_1 v_I}{2}\sqrt{4KI_O-K^2v_I^2}$$

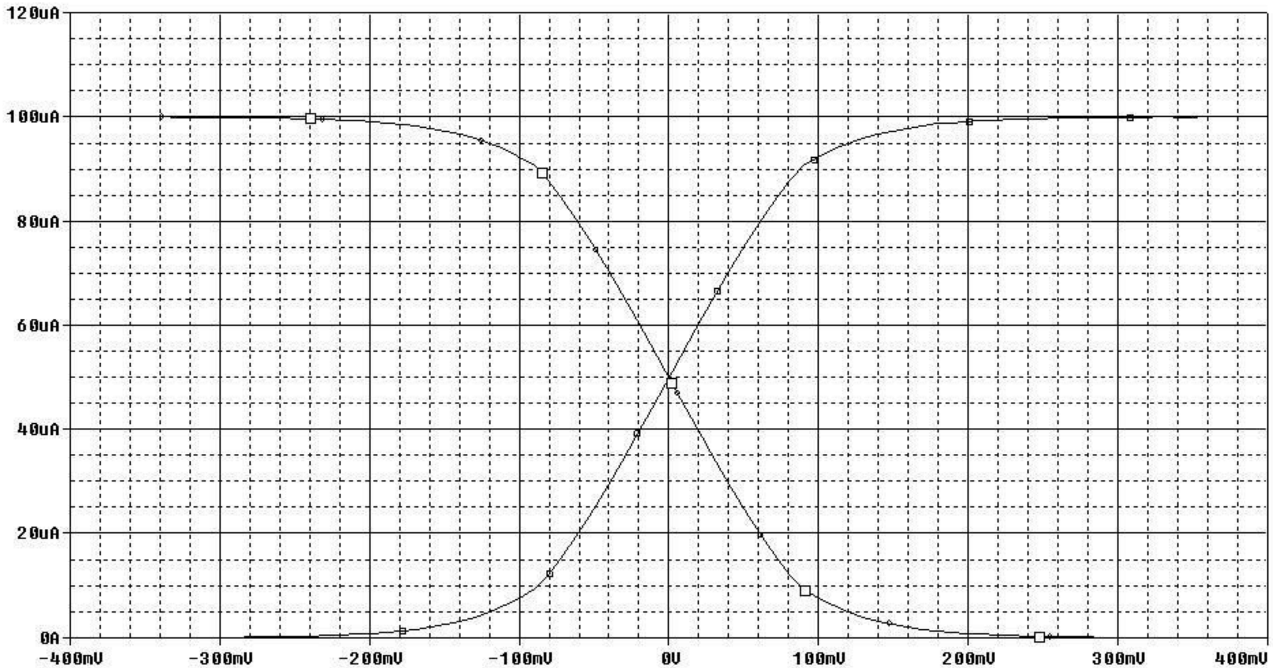
The Taylor series expansion of the output voltage is:

$$v_O(v_I) = -K^{1/2} I_O^{1/2} R_1 v_I + \frac{K^{3/2} R_1}{8 I_O^{1/2}} v_I^3 + \frac{K^{5/2} R_1}{128 I_O^{3/2}} v_I^5 + \ldots$$

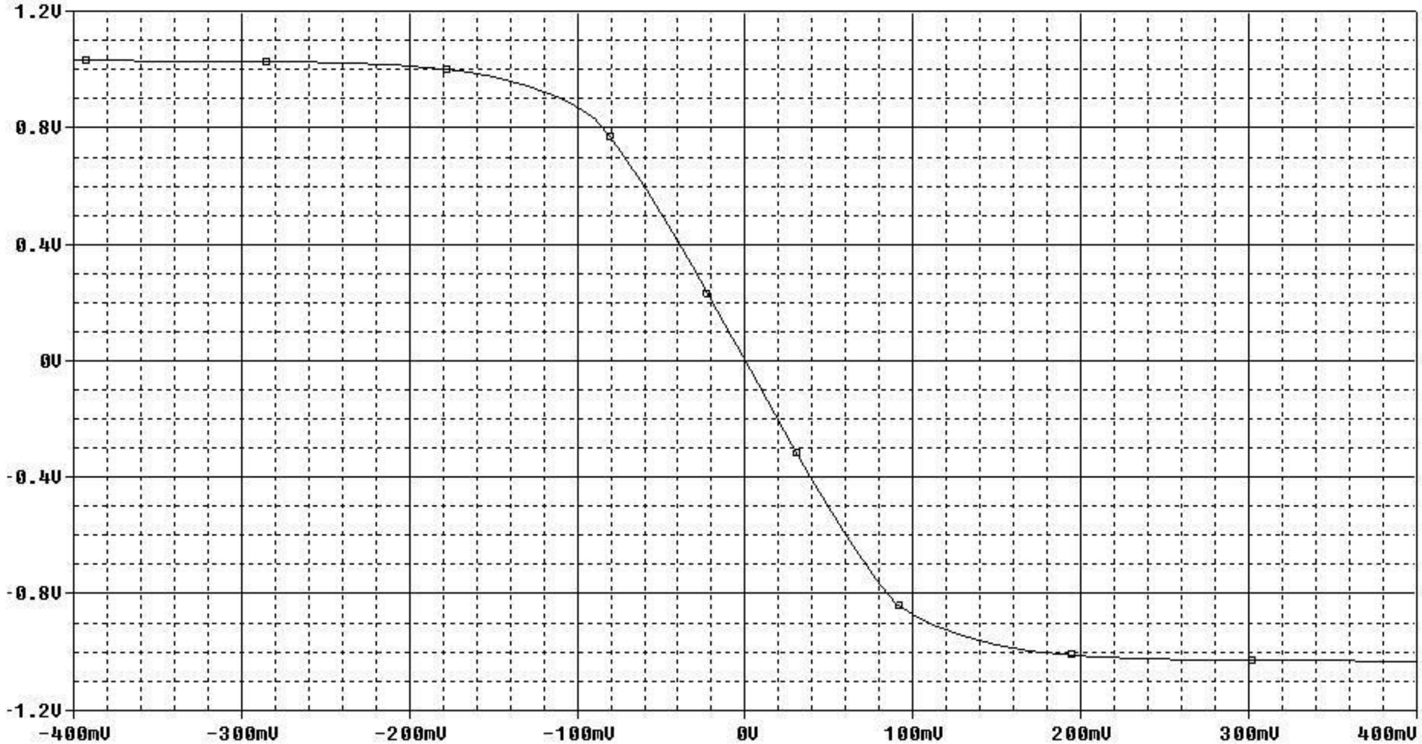
$$v_O(v_I) = a_1 v_I + a_3 v_I^3 + a_5 v_I^5 + \ldots$$

The differential mode gain is:

$$A_{dd} = a_1 = -R_1 \sqrt{K I_O}$$



$i_{D1}, i_{D2}(v_I)$ characteristics



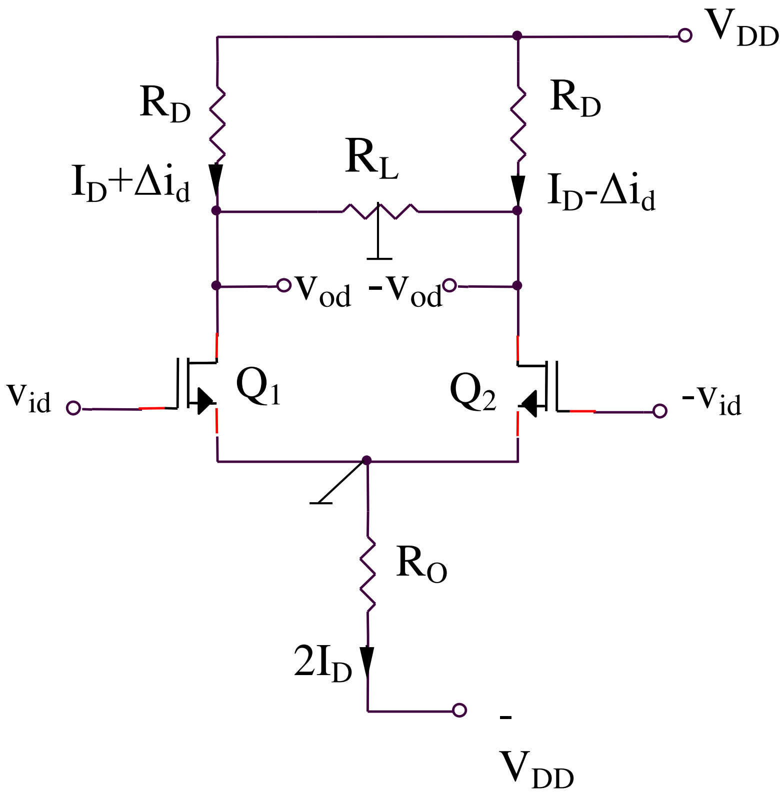
$v_O(v_I)$ characteristic

3.6.2. Small signal analysis

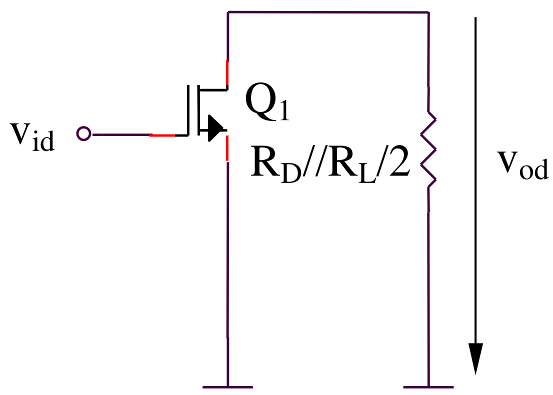
3.6.2. Small signal analysis

Determination of the small-signal gain: half circuit method

Differential mode ($v_{id} \neq 0$, $v_{ic} = 0 \Rightarrow v_{i1} = v_{id}$, $v_{i2} = - v_{id}$)
An additional load resistance (R_L) has been introduced.



(a)



(b)

Differential mode gain:

$$A_{dd} = \frac{v_{od}}{v_{id}} = -g_{m1}\left(R_D \,//\, \frac{R_L}{2} \right)$$

- symmetrical output:

$$A = \frac{2v_{od}}{2v_{id}} = A_{dd}$$

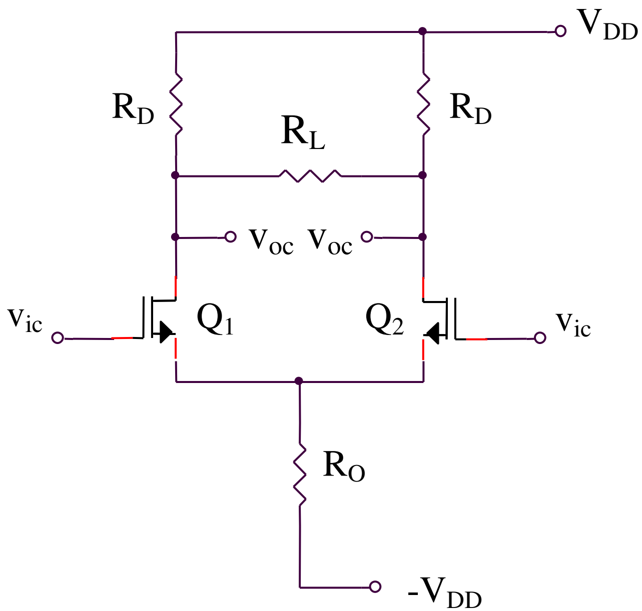
- non-symmetrical output:

$$A = \frac{v_{od}}{2v_{id}} = \frac{A_{dd}}{2}$$

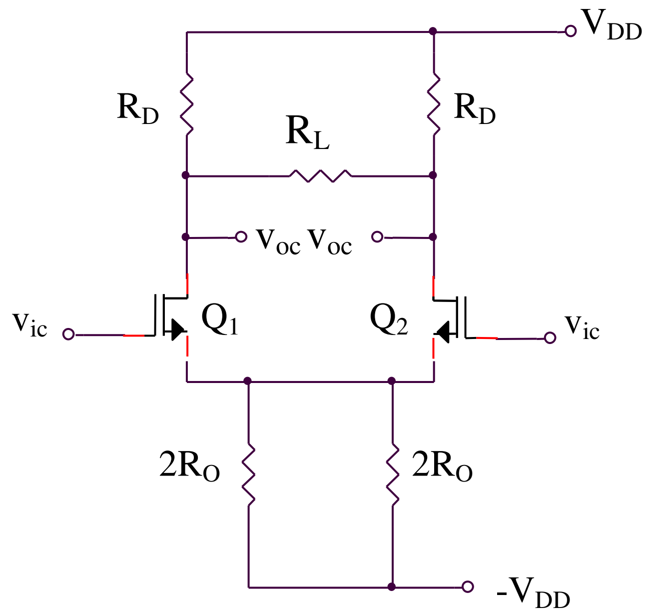
Differential input resistance:

$$R_{id} = \infty$$

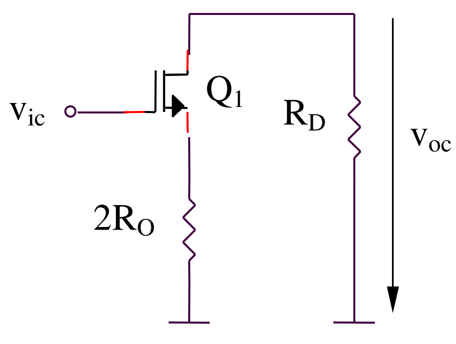
Common mode ($v_{ic} \neq 0$, $v_{id} = 0 \Rightarrow v_{i1} = v_{ic}$, $v_{i2} = v_{ic}$)



(a)



(b)



(c)

Common mode voltage gain:

$$A_{cc} = \frac{v_{oc}}{v_{ic}} = -\frac{g_{m1}R_D}{1 + g_{m1}2R_O} \cong -\frac{R_D}{2R_O}$$

Common mode input resistance:

$$R_{ic} = \infty$$

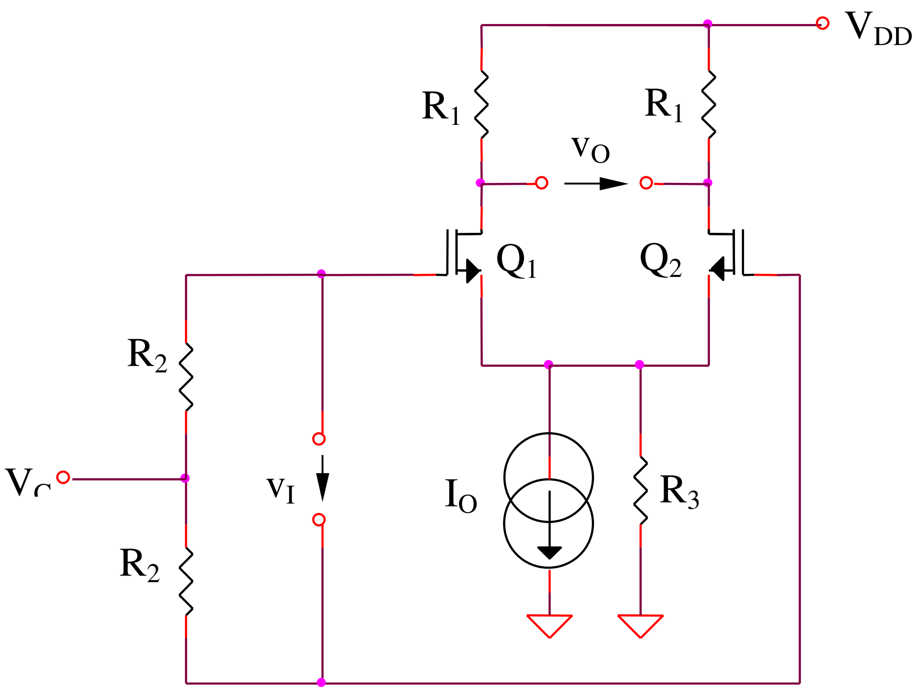
So:

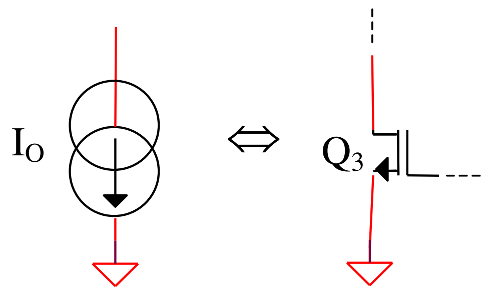
$$CMRR = \frac{2g_{m1}R_L R_O}{2R_D + R_L}$$

For increasing CMRR, it is necessary to increase R_O, by replacing the current source by a cascode current source.

3.6.3. Maximum range of the common-mode input voltage

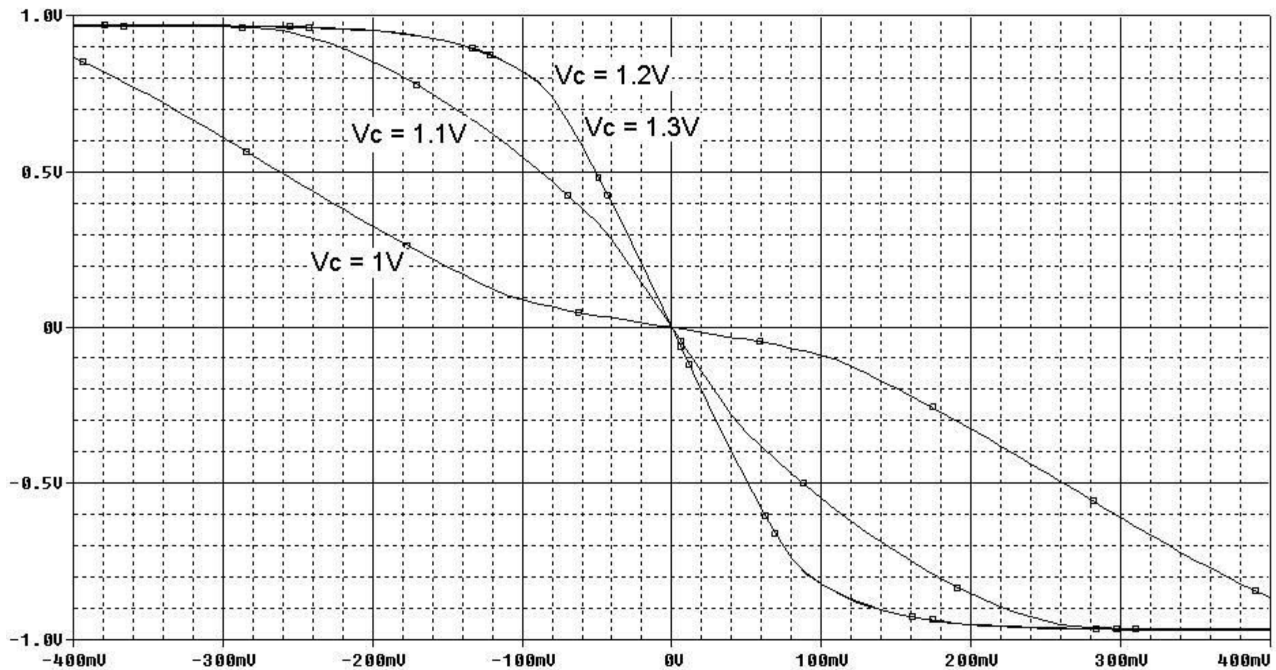
3.6.3. Maximum range of the common-mode input voltage





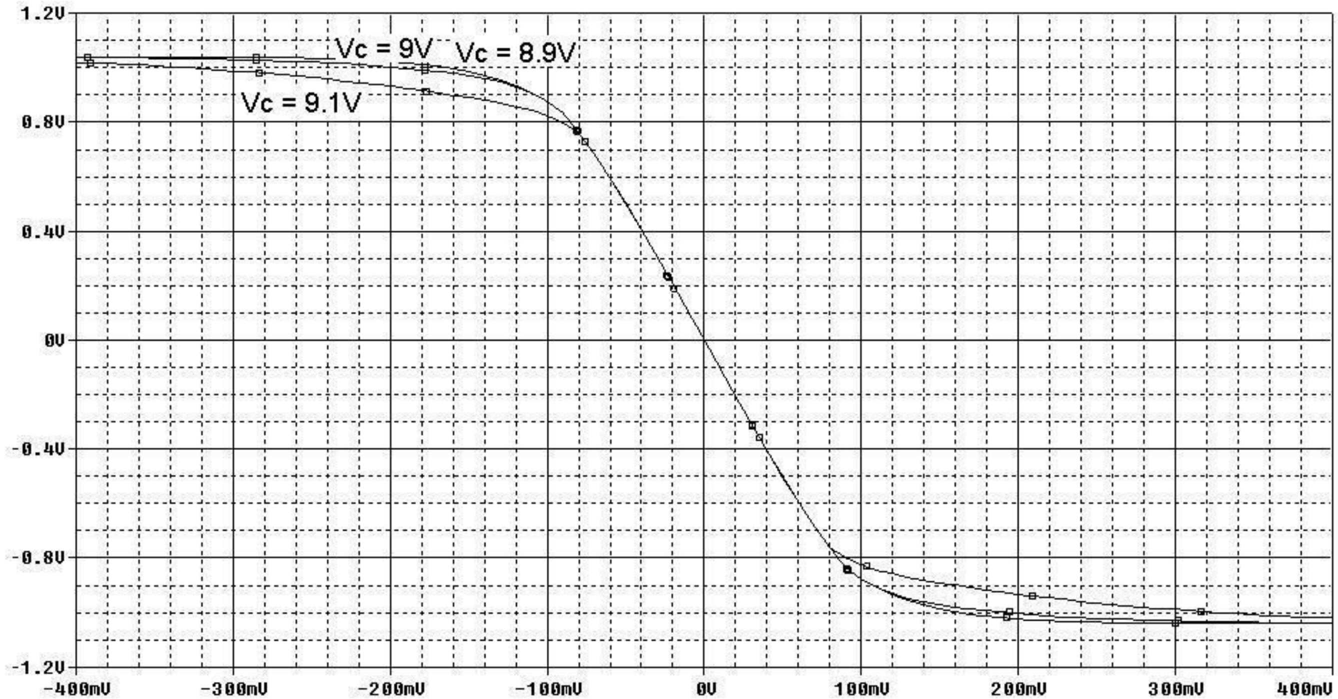
$$V_{C\min} = v_{GS1} + v_{DS3sat} = v_{GS1} + v_{GS3} - V_T = V_T + \left(\sqrt{2}+1\right)\sqrt{\frac{I_O}{K}}$$

$$V_{C\max} = V_{DD} - \frac{I_O R_1}{2} - v_{DS1sat} + v_{GS1} = V_{DD} - \frac{I_O R_1}{2} + V_T$$



$v_O(v_I)$ characteristics for multiples common-mode input voltages

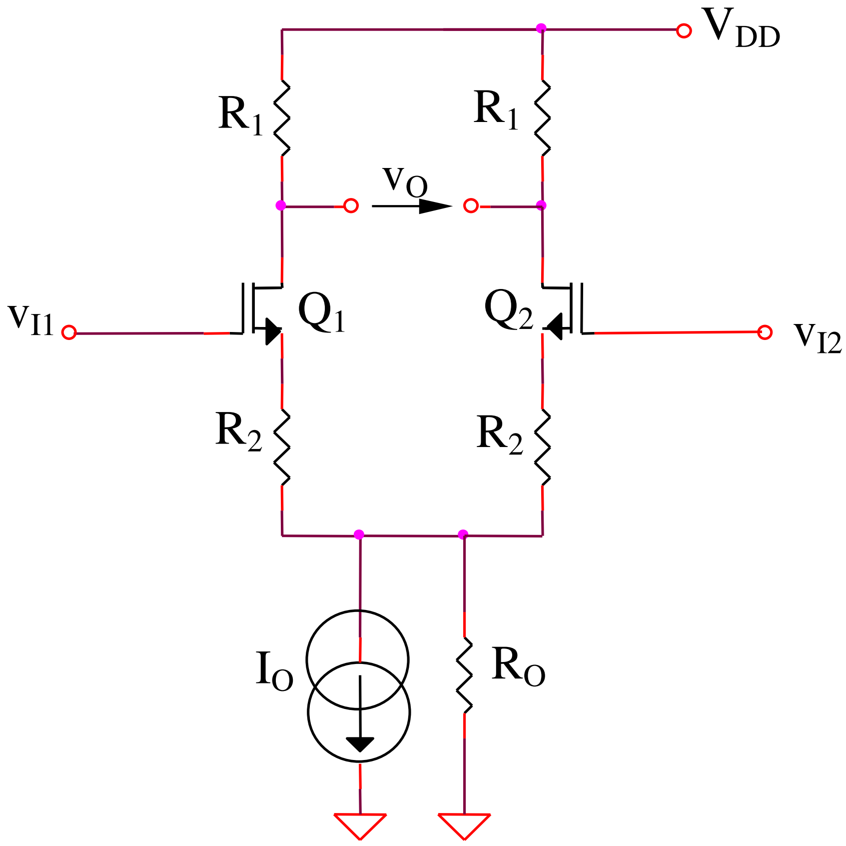
$$V_{C\,\mathrm{min}} \cong 1.2V$$



$v_O(v_I)$ characteristics for multiples common-mode input voltages

$$V_{C\max} \cong 9V$$

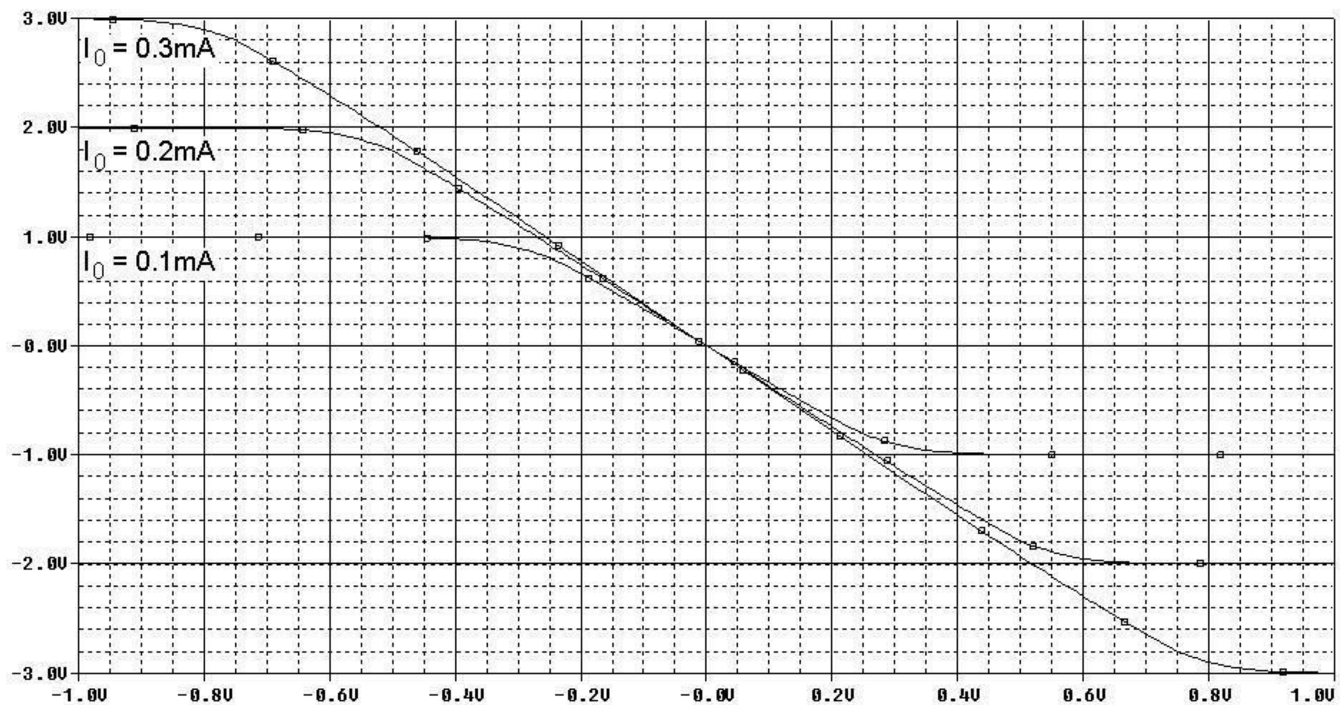
It is possible to increase the range of the differential input voltage for a linear operation of the circuit by inserting two resistors in emitters.



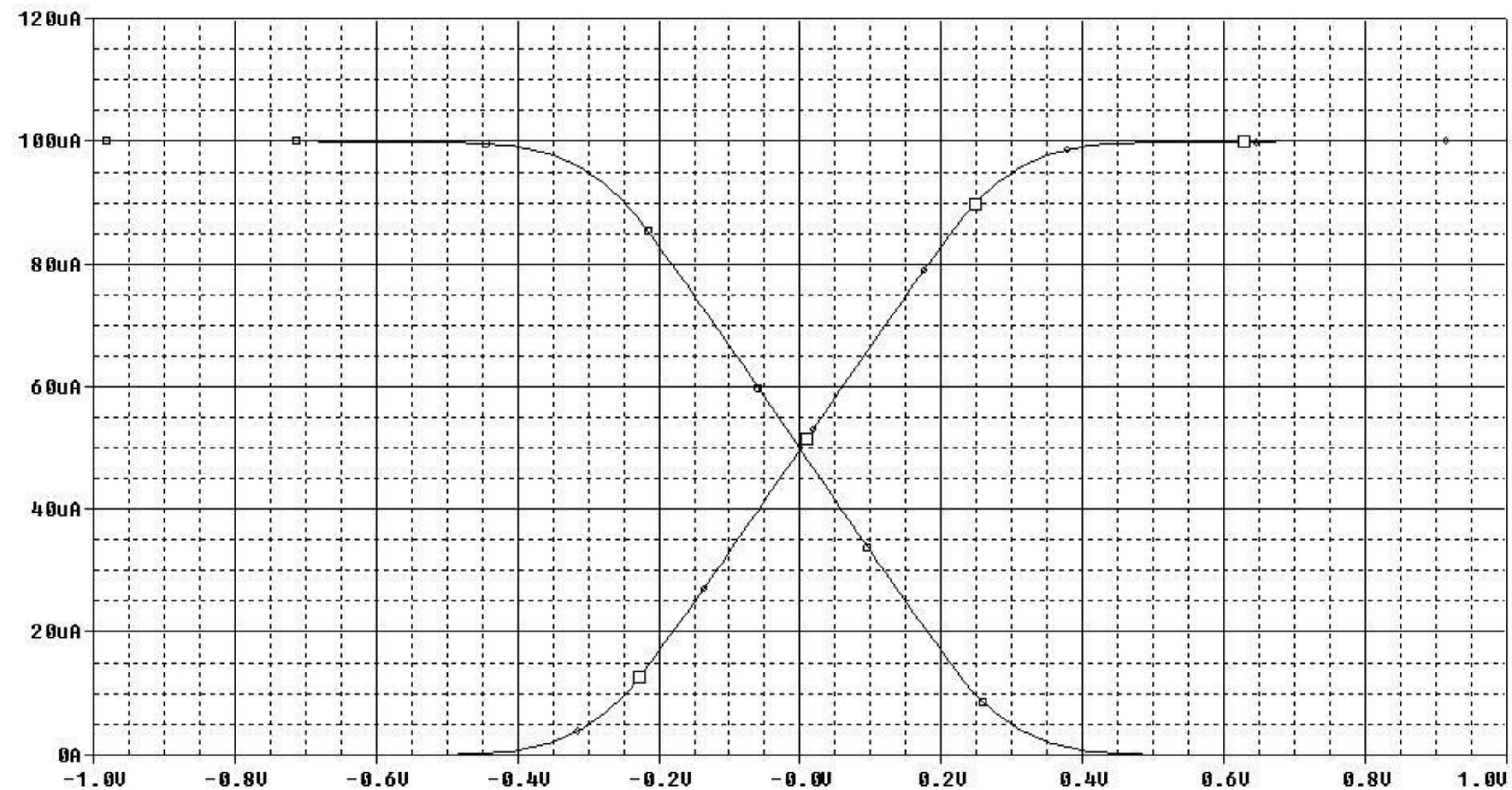
$$A_{dd} = -\frac{g_m R_1}{1 + g_m R_2} \qquad A_{cc} = -\frac{g_m R_1}{1 + g_m (R_2 + 2R_O)}$$

$$V_{C\min} = v_{GS1} + v_{DS3sat} + \frac{I_O R_2}{2} = v_{GS1} + v_{GS3} - V_T + \frac{I_O R_2}{2} = V_T + \left(\sqrt{2} + 1\right)\sqrt{\frac{I_O}{K}} + \frac{I_O R_2}{2}$$

$$V_{C\max} = V_{DD} - \frac{I_O R_1}{2} - v_{DS1sat} + v_{GS1} = V_{DD} - \frac{I_O R_1}{2} + V_T$$



$v_O(v_I)$ characteristics for multiple biasing currents

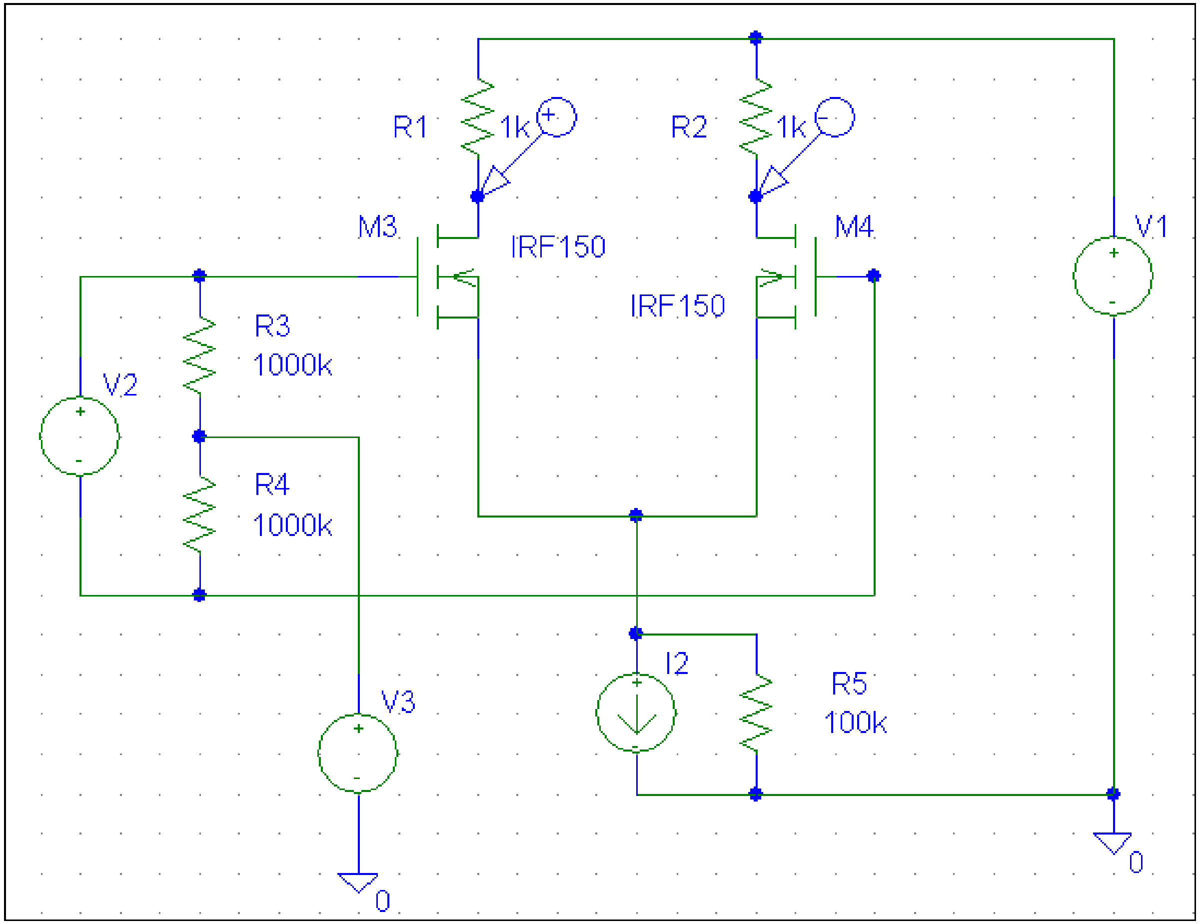


$i_{D1}, i_{D2}(v_I)$ characteristics

SIMULATIONS for CMOS differential amplifier
Differential-mode large signal analysis

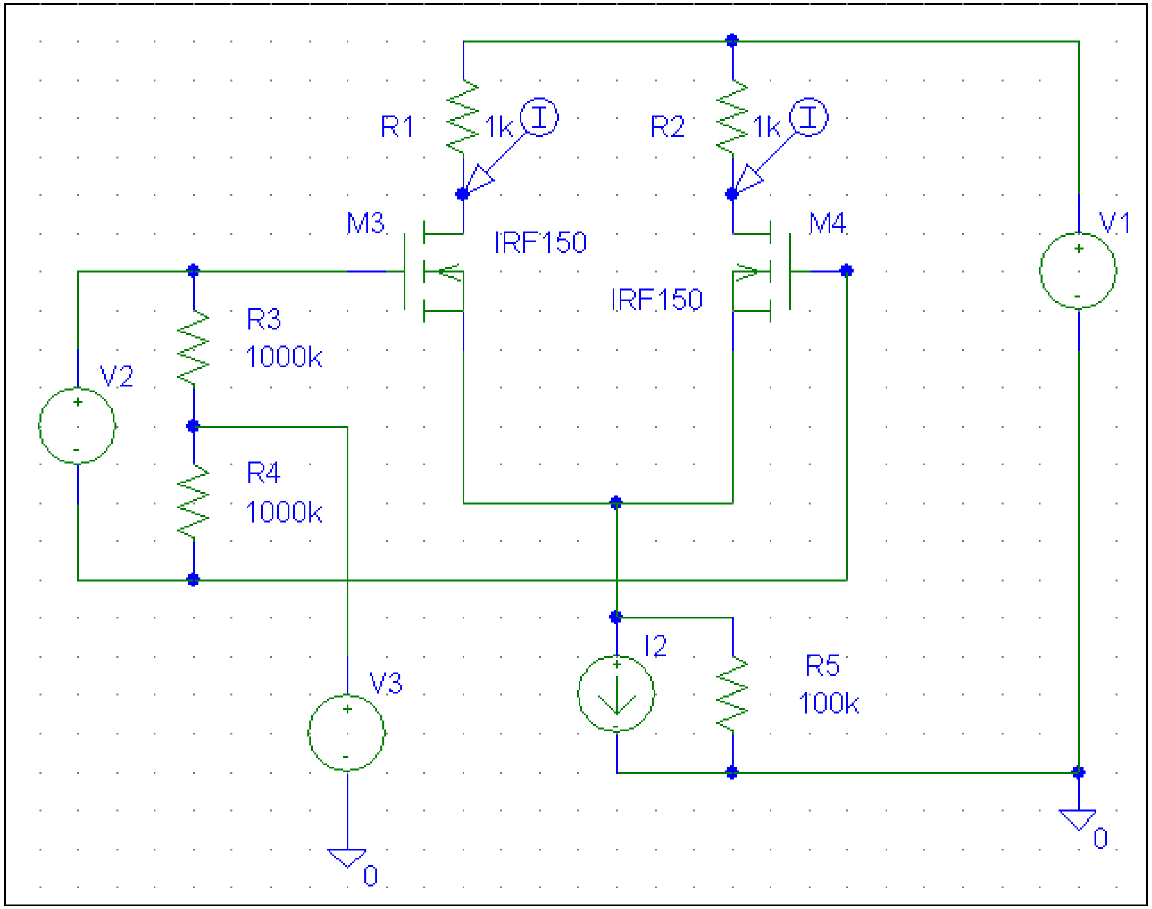
SIMULATIONS for CMOS differential amplifier
Differential-mode large signal analysis

SIM 3.7: V_O (V2)



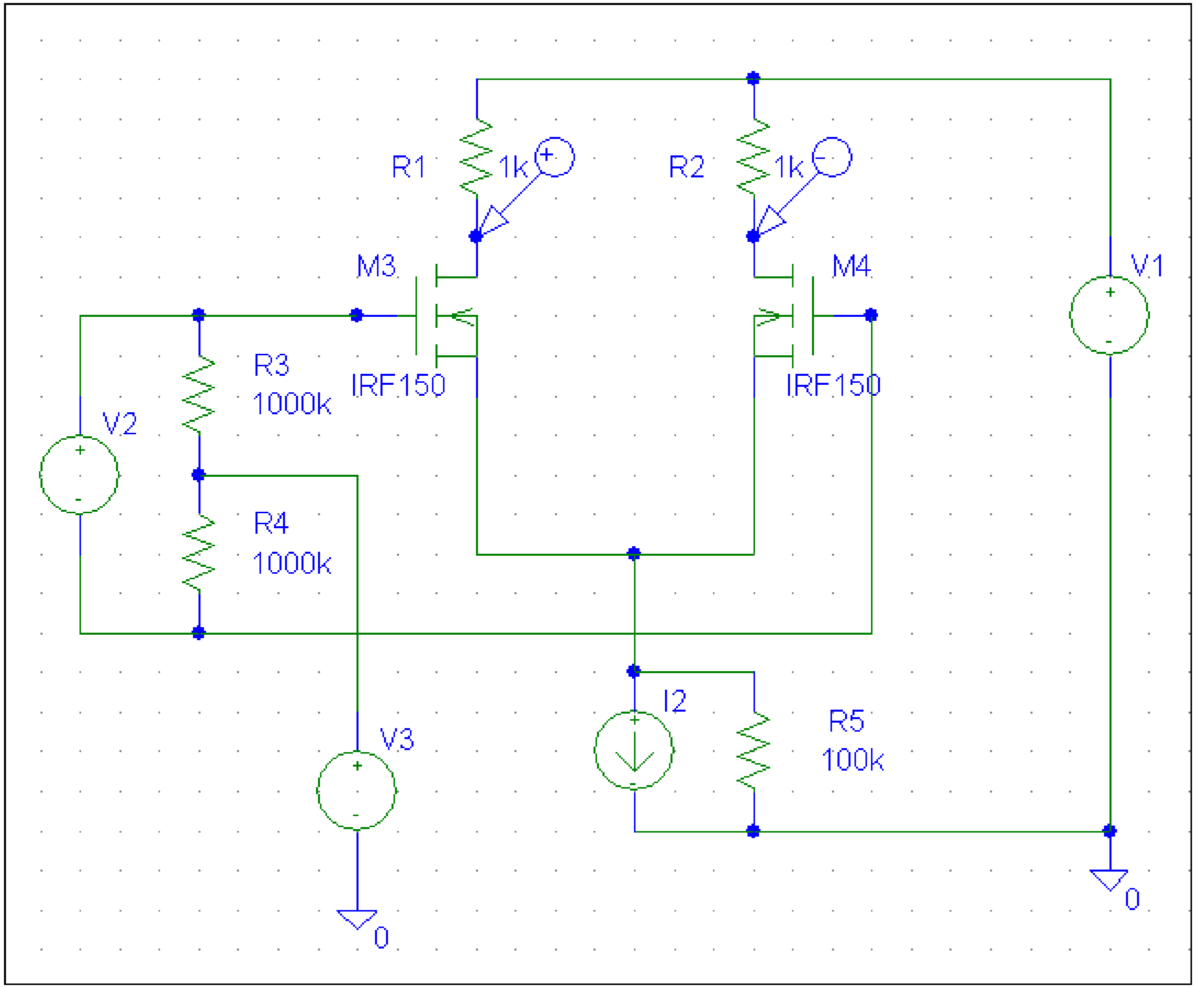
SIMULATIONS for CMOS differential amplifier
Differential-mode large signal analysis

SIM 3.8: i_{D1}, i_{D2} (V2)



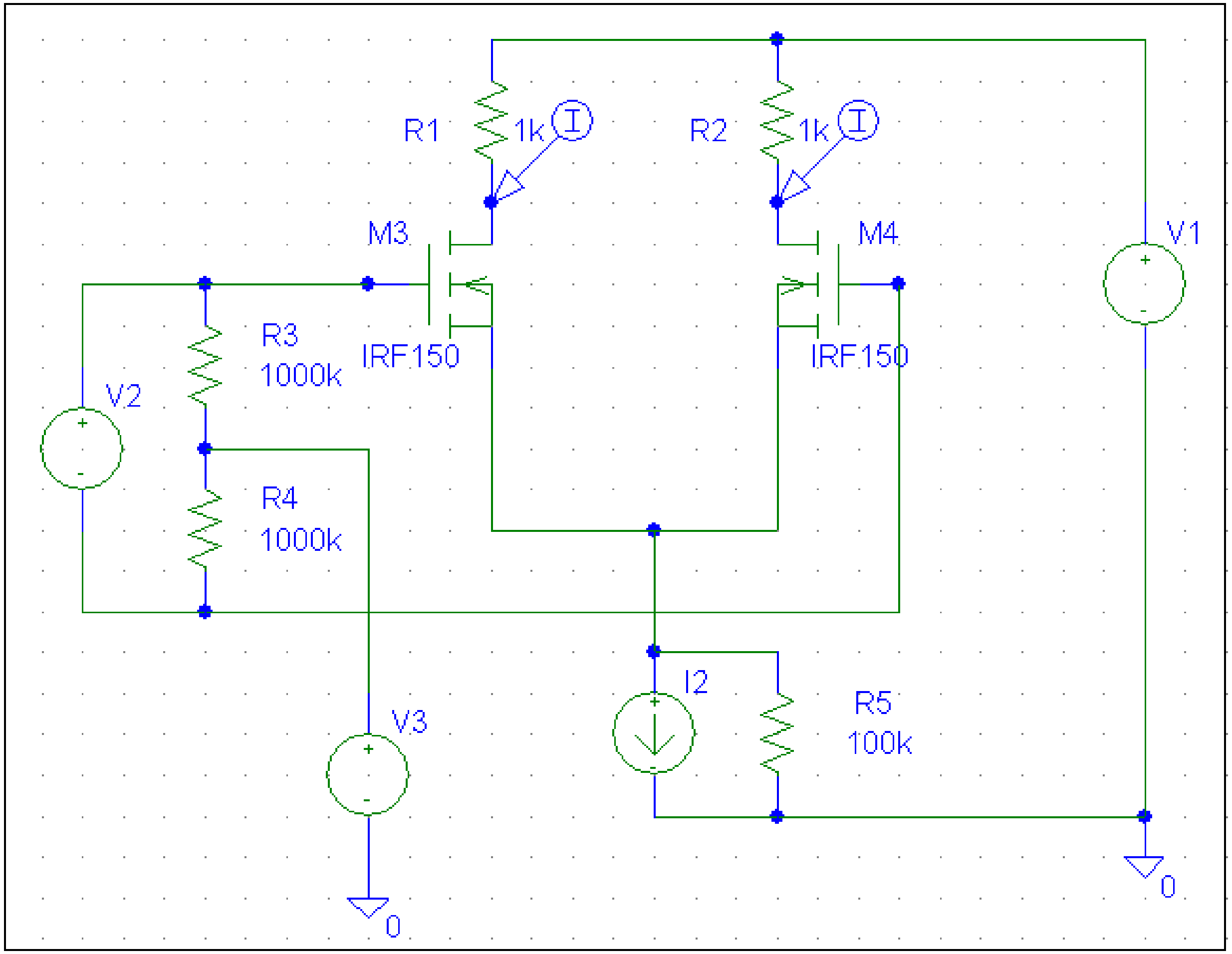
SIMULATIONS for CMOS differential amplifier
Differential-mode large signal analysis

SIM 3.9: V_O (V2), I2 - paramètre



SIMULATIONS for CMOS differential amplifier
Differential-mode large signal analysis

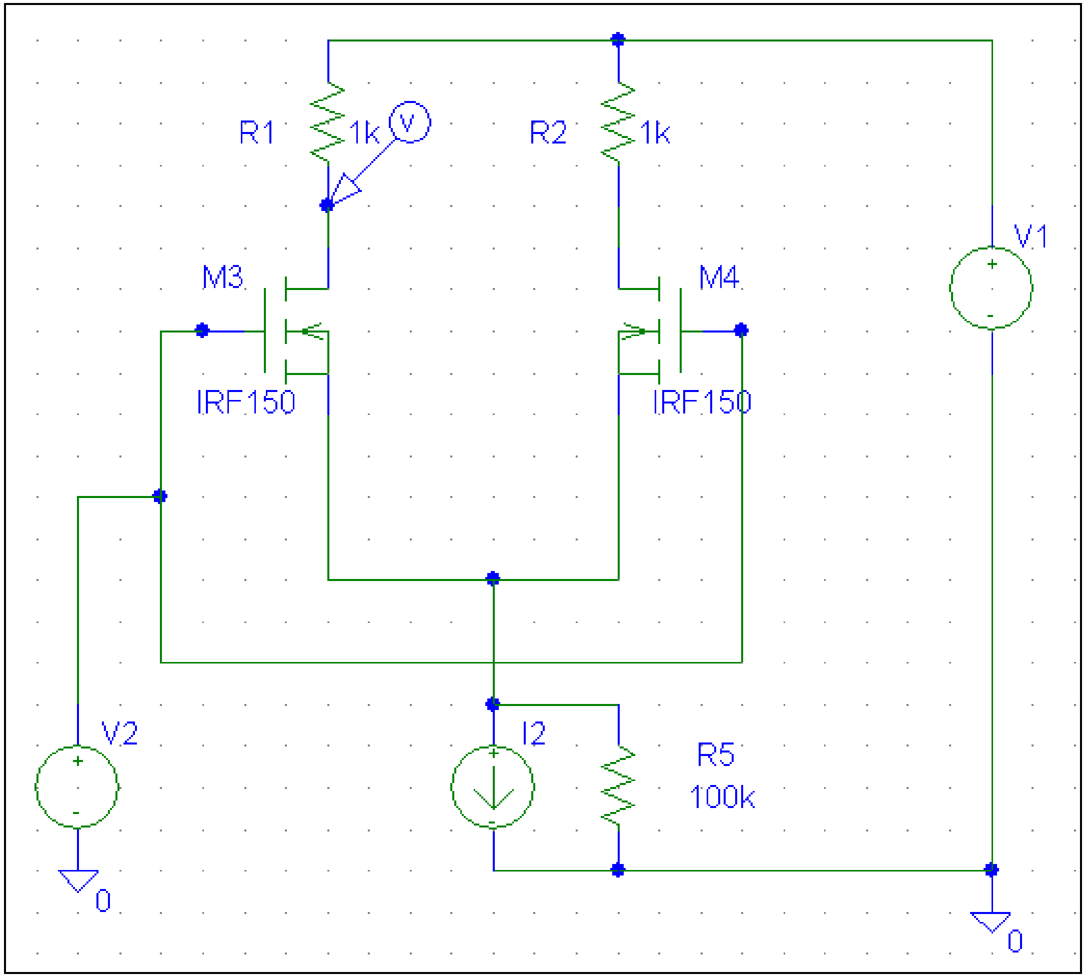
SIM 3.10: i_{D1}, i_{D2} (V2), I2 - paramètre



SIMULATIONS for CMOS differential amplifier
Common-mode large signal analysis

SIMULATIONS for CMOS differential amplifier
Common-mode large signal analysis

SIM 3.11: V_{C1} (V2)



3.6.4. Input offset voltage

3.6.4. Input offset voltage

If the two transistors are not identical, it is necessary to apply a input voltage (named input offset voltage) in order to obtain a null output voltage.

$$V_{IO} = v_{GS1} - v_{GS2} = (V_{T1} - V_{T2}) + \left(\sqrt{\frac{2i_{D1}}{K'(W/L)_1}} - \sqrt{\frac{2i_{D2}}{K'(W/L)_2}} \right)$$

$$V_{IO} = \Delta V_T + \sqrt{\frac{2(i_D + \Delta i_D/2)}{K'[(W/L) - \Delta(W/L)/2]}} - \sqrt{\frac{2(i_D - \Delta i_D/2)}{K'[(W/L) + \Delta(W/L)/2]}}$$

$$V_{IO} = \Delta V_T + \sqrt{\frac{2i_D}{K'(W/L)}} \left[\sqrt{1 + \frac{\Delta i_D}{2i_D} + \frac{\Delta(W/L)}{2(W/L)}} - \sqrt{1 - \frac{\Delta i_D}{2i_D} - \frac{\Delta(W/L)}{2(W/L)}} \right]$$

Similar with bipolar circuit, it results:

$$V_{IO} = \Delta V_T + \frac{V_{GS} - V_T}{2} \left[\frac{\Delta i_D}{i_D} + \frac{\Delta(W/L)}{(W/L)} \right]$$

But:

$$\left(i_D + \frac{\Delta i_D}{2}\right)\left(R - \frac{\Delta R}{2}\right) = \left(i_D - \frac{\Delta i_D}{2}\right)\left(R + \frac{\Delta R}{2}\right)$$

equivalent with:

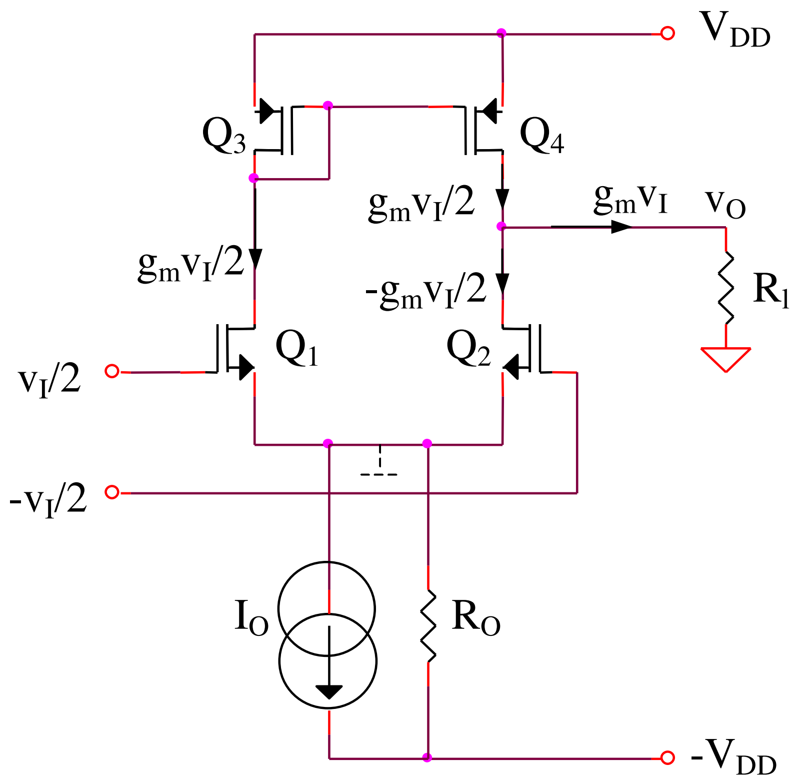
$$\frac{\Delta i_D}{i_D} = \frac{\Delta R}{R}$$

It results:

$$V_{IO} = \Delta V_T + \frac{V_{GS} - V_T}{2}\left[\frac{\Delta R}{R} + \frac{\Delta(W/L)}{(W/L)}\right]$$

3.6.5. Active load differential amplifier

3.6.5. Active load differential amplifier

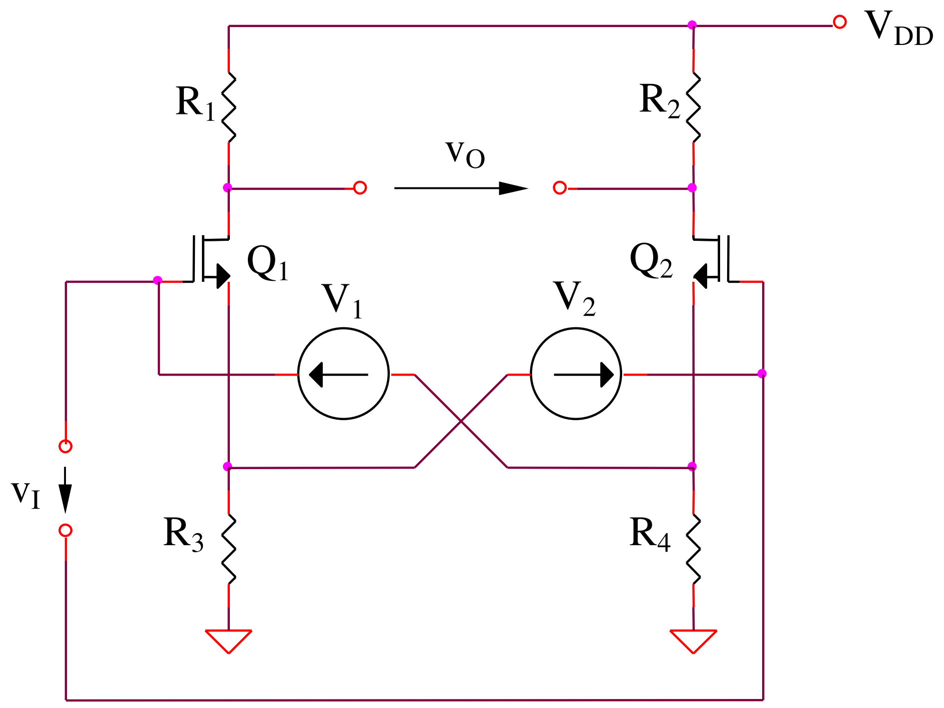


$$A_{dd} = g_m\left(r_{ds2} // r_{ds4} // R_l\right)$$

$$A_{dd}\Big|_{R_l \to \infty} = g_m\left(r_{ds2} // r_{ds4}\right) = g_m \frac{r_{ds}}{2} = \frac{1}{2\lambda}\sqrt{\frac{K}{I_O}}$$

3.6.6. Differential amplifier with the constant sum of gate-source voltages

3.6.6. Differential amplifier with the constant sum of gate-source voltages



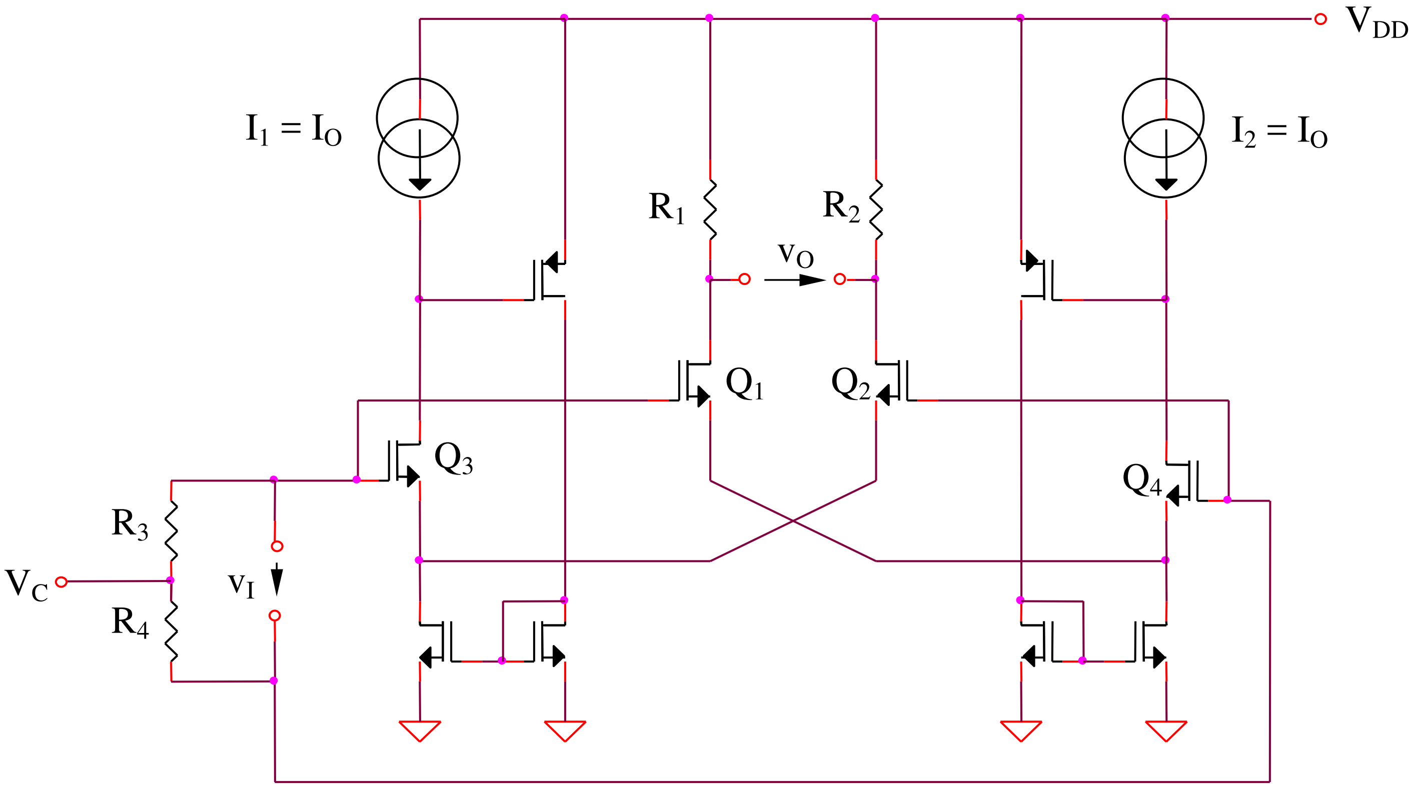
$$i_{D1} = \frac{K}{2}\left(v_{GS1} - V_T\right)^2 \qquad i_{D2} = \frac{K}{2}\left(v_{GS2} - V_T\right)^2$$

$$v_O = R_1\left(i_{D2} - i_{D1}\right) = \frac{KR_1}{2}\left(v_{GS2} - v_{GS1}\right)\left(v_{GS2} + v_{GS1} - 2V_T\right)$$

$$v_I = V_1 - v_{GS2} = v_{GS1} - V_2 \;\Rightarrow\; \begin{cases} v_{GS1} - v_{GS2} = 2v_I \\ v_{GS1} + v_{GS2} = 2V \end{cases} \Rightarrow$$

$$\Rightarrow \begin{cases} v_O = -2KR_1\left(V - V_T\right)v_I \\ A_{dd} = \dfrac{v_O}{v_I} = -2KR_1\left(V - V_T\right) \end{cases} \qquad V_1 = V_2 = V$$

Possible implementation



$$V_1 = V_2 = V_{GS3} = V_{GS4} = V_T + \sqrt{\frac{2I_O}{K}} \qquad \Rightarrow A_{dd} = -2R_1\sqrt{2KI_O}$$