Călin BÎRĂ

==========

Digital Electronics by Example

When Hardware greets Hardware

Preface

This book is an educational book and provides examples and exercises for the students in 2nd year of bachelor's degree path, regarding the Digital Electronics topic.

Chapter one provides an introduction into analog and digital signals and systems and is similar to the introduction in [1]

Chapter two starts with exercises regarding 0-loop circuits.

Chapter two and three are an introduction into basic digital and analog components, while chapter four is a discussion regarding complexity. Finally, chapter five is a walkthrough on design and implementation of a few mixed-signal systems used in real-life. This book uses a lot of pictures, and instead of citing each of them with their source, I opted to create a table of figures, where I give credit where credit is due.

Table of Contents

Preface 2
Table of Contents 3
List of Figures 5
List of Tables 7
List of Acronyms 8
1. Brief Introduction to Digital Circuits and Programming 13
1.1 Analog signals 13
1.2 Digital signals 13
1.3 Digit, number, and radix 15
1.4 Digital systems 16
1.5 The advantages of using digital systems 17
2. The FPGA (Field Programmable Gate Array) 18
2. Zero-loop systems 22
2.1 Prerequisites 22
2.1.1 Binary and Boolean Logic 22
2.1.2 Digital Gates 23
2.1.3 Complexity in digital circuits 24
2.1.4 Complexity classes 25
2.1.4 Verilog syntax 27
2.1.5 VHDL syntax 29
2.4 Theory & Exercises 32
2.4.1 Multiple-input gates 32
2.4.2 Elementary multiplexer 34
3. One-loop systems 40
4. Two-loop systems (automata) 40
4.1 Prerequisites 40
4.2 Theory 40
4.3 TODO: other exercises 40
Figure References 47
References 49

List of Figures

Figure 1. A digital signal (as a result of both sampling and quantization processes) 13
Figure 2. A time-sampled signal (as a result of sampling process) 14
Figure 3. A value-sampled signal (as a result of quantization process) 14
Figure 4. Analog to digital conversion, digital processing and digital to analog conversion example 17
Figure 5. Generic FPGA Architecture Overview 18
Figure 6. Xilinx CLB. Blue blocks are multiplexers, violet blocks are FFs and dark-green blocks are LUTs (look-up tables) 18
Figure 7. FPGA development flow 19
Figure 8. The Nexys 4 DDR FPGA board 20
Figure 9. Nexys 4 DDR board features 20
Figure 10. GPIO devices on the Nexys4 DDR FPGA board 21
Figure 11. NOT gate (“inverter”) made of one pMOS (top) and one nMOS (bottom) transistor 23
Figure 12. ANSI / IEC [5] (right) and MIL-STD-806B [6] (left) symbols foremost common 7/16 dual-input logic gates (elementary), with their names. 23
Figure 13. The truth tables for the most commonly used logic gates. 24
Figure 14. Representing a g(n) function which asymptotically bound f(n) function. 25
Figure 15. The O-notation complexity increases with the number of elements processed. O(1) and O(logn) are usually excellent complexities, O(n) is fair, and O(n*logn) is usually considered almost decent in algorithms and circuits 25
Figure 16. A 16-input AND gate built from 2-input AND gates. 26
Figure 17. Verilog syntax cheat sheet (1/2) 27
Figure 18. Verilog syntax cheat sheet (2/2) 28
Figure 19. VHDL cheat sheet (1/2) 29
Figure 20. VHDL cheat sheet (2/2) 30
Figure 21. 2-input AND gate 31
Figure 22. Verilog code (dataflow) for a 2-input AND gate 31
Figure 23. Verilog code (dataflow) for a 2-input AND gate 31
Figure 24. 4-input AND gate from 2-input AND gates (dataflow) 32
Figure 25. Verilog description for 4-input AND (dataflow) 32
Figure 26. VHDL description for 4-input AND (dataflow) 32
Figure 27. 4-input AND gate from 2-input AND gates (structural) 33
Figure 28.Verilog description of 4-input AND gate from 2-input AND gates (structural) 33
Figure 29. VHDL description of 4-input AND gate from 2-input AND gates (structural) 34
Figure 30. MUX2 implemented with one NOT, two AND, one OR gate(s) 34
Figure 31. LUT-based implementation of elementary mux, in FPGA 35
Figure 32. Verilog description of elementary MUX 35

List of Tables

Table 1. Multiples of bits / bytes according to JEDEC [2]. IEC 80000-13 standard changes the name for the power of two, by inserting a “bi” in the name: Kibibyte, Mebibyte, Gibibyte. 15
Table 2. A (general) logic operation’s truth table 22
Table 3. Truth tables for AND, OR and NOT operations 22
Table 4. Truth tables for AND, OR and NOT operations (seen as 1-bit operations) 22

List of Acronyms

AACS	Advanced Access Content System
AC	Alternative Current
ACK	Acknowledge
ADC	Analog to digital converter
AES	Advanced Encryption Standard
AGM	Absorbent Glass Mat
AMD	Advanced Micro Devices
ANSI	American National Standards Institute
ARPA	Advanced Research Projects Agency
ARPANET	Advanced Research Projects Agency Network
ASIC	Application Specific Integrated Circuit
BIOS	Basic Input-Output System
BJT	Bipolar Junction Transistor
BOD	Brown-out detect
CBC	Cipher Block Chaining
CD	Compact Disk
CDIP	Ceramic Dual Inline Package
CERN	Conseil Européen pour la Recherche Nucléaire / European Council for Nuclear Research
CFB	Cipher Feedback Mode
CMOS	Complementary Metal-Oxide Semiconductor
COBOL	Common Business-Oriented Language
CPHA	Clock Phase
CPOL	Clock Polarity
CPU	Central Processing Unit
CRT	Cathode-Ray Tube
CS	Chip Select
CSNET	Computer Science Network
CTFT	Continuous Time Fourier Transform
CTR	Counter
CUDA	Compute Unified Device Architecture
CV	Computer Vision
DAC	Digital to Analog Converter
DC	Direct Current
DDR	Double Data Rate
DES	Data Encryption Standard
DHCP	Dynamic Host Configuration Protocol
DIP	Dual In-line Package
DNA	Deoxyribonucleic Acid
DNS	Domain Name Service

DRAM	Dynamic Random Access Memory
DUT	Device Under Test
EB	Exabyte
ECB	Electronic Code Book
ECC	Error Correction Code
EMES	Engineering of Modern Electric Systems
FET	Field-Effect Transistor
FIFO	First-In First-Out
FIPS	Federal Information Processing Standard
FM	Frequency Modulation
FTP	File Transfer Protocol
GB	Gigabyte
GHz	Gigahertz
GND	Ground
GP	General Purpose
GPIO	General Purpose Input/Output
GPU	Graphical Processing Unit
GUI	Graphical User Interface
HD	High Definition
HDD	Hard Disk Drive
HDL	Hardware Description Language
HTML	Hypertext Markup Language
I2C	Inter-integrated circuit
IC	Integrated circuit
ICPSC	International Conference on Signal Processing and Communication
IDE	Integrated development environment
IEC	International Electrotechnical Commission
IEEE	Institute of Electrical and Electronics Engineers
IR	Infrared
ISO	International Organization for Standardization
JBOD	Just a Bunch of Disks
JEDEC	Joint Electron Device Engineering Council
JS	JavaScript
KB	Kilobyte
kHz	Kilohertz
LED	Light-emitting diode
LIDAR	Light Detection and Ranging
LSB	Least Significant Bit/Byte
MATLAB	Matrix Laboratory
MB	Megabyte
MCU	Microcontroller Unit

MHz	Megahertz
MIL-STD	Military Standard
MIT	Massachusetts Institute of Technology
MOhm	Megohm
MOS	Metal-Oxide Semiconductor
MSB	Most Significand Bit/Byte
MW	Megawatt
NACK	Not Acknowledge
NAND	Not AND
NIST	National Institute of Standards and Technology
NO	Normal Open
NOM	Nominal
NOR	Not OR
NP	Non-polynomial
NSF	National Science Foundation
NTC	Negative Temperature Coefficient
NTP	Network Time Protocol
NVM	Non-Volatile Memory
OFB	Output Feedback Mode
OOK	On/Off Keying
OP	Operation
OSI	Open Systems Interconnection Model
OTP	One Time Password
OUT	Output
PB	Petabyte
PC	Personal Computer
PCB	Printed Circuit Board
PCBC	Propagating or Plaintext Cipher-Block Chaining
PCI	Peripheral Component Interconnect
PDIP	Plastic Dual Inline Package
PHP	PHP: Hypertext Preprocessor
PIR	Passive Infrared
PN	Part Number
PTC	Positive Temperature Coefficient
PTP	Picture Transfer Protocol
QSPI	Quad SPI
R,G,B	Red, Green, Blue
RADAR	Radio Detection and Ranging
RAID	Redundant Array of Independent Disks
RAM	Random Access Memory
RC	Remote Control

RDS(on)	Resistance from drain to source, when in on state
RF	Radio Frequency
RFC	Request for Comments
RFID	Radio Frequency Identification
RGB	Red Green Blue
RH	Relative humidity
RMS	Root Means Square
RNA	Ribonucleic Acid
RSA	Rivest-Shamir-Adleman (Encryption)
RX	Receiver or reception
SAR	Successive approximative register
SATA	Serial Advanced Technology Attachment
SCK	Serial Clock
SCL	Serial Clock
SCR	Silicon controlled rectifier
SD	Secure Digital
SDA	Serial Data
SDRAM	Synchronous Dynamic Random Access Memory
SFTP	Secure File Transfer Protocol
SMD	Surface Mount Device
SNTP	Simple Network Time Protocol
SOIC	Small Outline Integrated Circuit
SPDT	Single Pole Double Throw
SPI	Serial Peripheral Interface
SPST	Single Pole Single Throw
SQL	Structured Query Language
SRAM	Static Random Access Memory
SS	Slave Select
SSD	Solid State Drive
SSH	Secure Shell
STFT	Short Term Fourier Transform
TB	Terabyte
TCP	Transmission Control Protocol
TCR	Temperature Coefficient of Resistance
TDP	Thermal Design Power
THT	Through Hole Technology
TIOBE	The Importance Of Being Earnest
TTL	Transistor-to-transistor logic
TV	Television
TVS	Transient Voltage Suppressors
TWI	Two Wire Interface

TX	Transmitter / Transmission
UART	Universal Asynchronous Receiver/Transmitter
UDIMM	Unbuffered Dual In-Line Memory Module
UDP	User Datagram Protocol
UHF	Ultra-High Frequencies
URL	Uniform Resource Locator
US	United States
USA	United States of America
USART	Universal Synchronous/Asynchronous Receiver/Transmitter
USB	Universal Serial Bus
UV	Ultraviolet
V	Volt
VHDL	VHSIC Hardware Description Language
VHF	Very High Frequency
VI	Input Voltage
VIH	Input Voltage (high, minimum)
VIL	Input Voltage (low, maximum)
VO	Output Voltage
VOH	Output Voltage (high, minimum)
VOL	Output Voltage (low, maximum)
WAN	Wide-Area Network
WDT	Watchdog Timer
WWW	World-Wide Web
XOR	Exclusive OR
YB	Yottabyte
ZB	Zettabyte

1. Brief Introduction to Digital Circuits and Programming

This chapter is similar to the first chapter in [1] and presents an introduction into digital signals and systems. There are advantages of converting analog signals into digital signals and back, otherwise one would not go through the trouble and cost of the conversion. These reasons will be highlighted at the end of this chapter.

1.1 Analog signals

All the studied systems in high-school's physics classes were composed from analog equipment/devices (voltage supplies, current supplies, resistors, capacitors, inductors, lightbulbs etc.). They are circuits where, for example, the voltage varies continuously within some limits. A default system is an analog audio amplifier, which takes an analogue audio signal, amplifies it (keeps the shape, but delivers more power from the supply) and sends it to the speakers. Analogue signals are hard to store and process, so lately, digital signals are used increasingly.

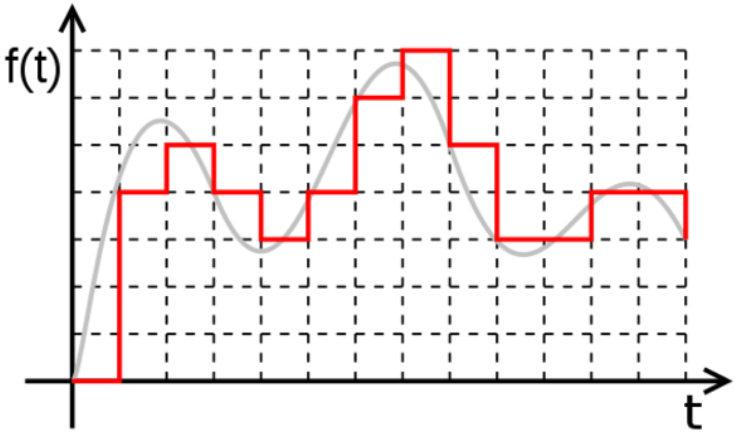


Figure 1. A digital signal (as a result of both sampling and quantization processes)

1.2 Digital signals

A digital signal is a signal which is discrete (as opposed to continuous) in both time and value. To create a time-discrete signal, one samples a continuous one. To create a value-discrete signal, one quantizes a continuous one.

The number of samples taken in a unit of time is called sampling rate (e.g., 44100 Hz == samples per second, CD-quality). The number of bits (0 or 1 symbols) required to express

the amplitude is linked directly to the number of quantization steps (e.g., 16-bit for 2 to the power of 16 = 65536 steps, in the case of CD-audio quality)

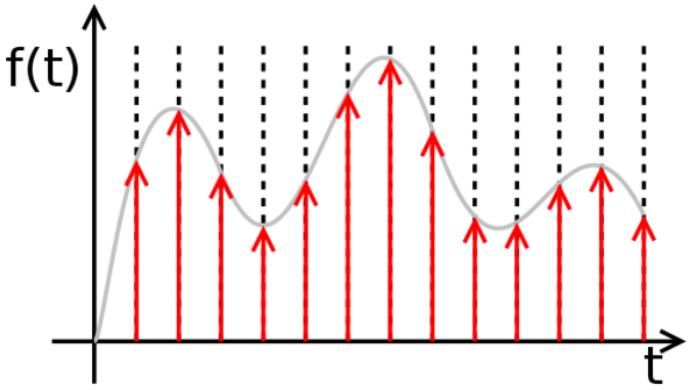


Figure 2. A time-sampled signal (as a result of sampling process)

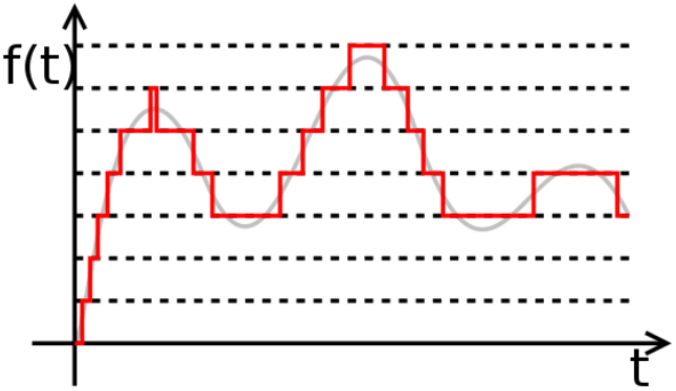


Figure 3. A value-sampled signal (as a result of quantization process)

Digital signals are used because their expression uses numbers, which allows easy storage, copying (without loss) and processing. Immunity to noise can be obtained using mathematical instruments like error-detection and error-recovery processes. In addition, the quality (how similar it looks to the source analogue signal) can be chosen as a compromise. The more quantization steps we use (e.g. infinite) the more accurate the value is to the source signal's value: however, these systems are usually used for the comfort of human life, so the trade-off will take into consideration human hearing or human sight etc. which will not push the quantization step too high (e.g. audio signals are good enough when using 64k steps, that is 16-bits per sample; video signals are good enough when colors are represented with 256 steps of Red, Green and Blue, therefore 3x 8-bits are enough for a pixel) Regarding the recovery of a continuous signal from the time-sampled signal, we have the sampling theorem which demonstrates that we can fully recover the original, as long as the sampling

rate is at least twice the maximum frequency contained in the original signal. For example, if one wants to recover up to 22 kHz audio signals (more than what the common human ear can hear), one should use 44 kHz sampling rate.

1.3 Digit, number, and radix

A radix-10 number uses a dictionary of 10 symbols (the ten digits) to express any number. For example, number 123 is made of 1 * 100 + 2 * 10 + 3. The radix of 10 is not the only known radix but is the most used by humans (arguably because we have ten fingers and can count easily using them). However, to use radix of 10, one must distinguish between 10 different symbols (0-9). Digital electronics use radix of 2 because it is easier to distinguish between only two symbols, therefore it is easier to store information in this form. The trade-offs that same number expressed in radix of 10 is around 3.5 times shorter that a radix of 2. For example, 9 is expressed in radix 2 with the sequence 1001, the number 127 is 11111111 etc. The symbols available for the radix of 2 are 0 and 1, and they are called BInary digiTS, in short bits. Using 2 digits we can express numbers from 0 to 99 (that is, 100 different numbers). Using 2 bits we can express numbers from 0 to 3 (that is, 4 different numbers). Most common radices are 2 (binary), 8 (octal), 16 (hex), 10 (dec) and 256. We will mark numbers in radix 2, as prefixed with 0b e.g.: 0b1001 is number 9 in radix 10. The hexadecimal number will be prefixed with 0x e.g.: 0x10 is 16 in radix 10.

Table 1. Multiples of bits / bytes according to JEDEC [2]. IEC 80000-13 standard changes the name for the power of two, by inserting a "bi" in the name: Kibibyte, Mebibyte, Gibibyte.

Memory Unit (JEDEC)	**Memory unit (IEC)**	**Description**
Bit	Bit	Binary Digit 1 or 0
Kbit	Kibibit	1024 bits
Mbit	Mebibit	1024 Kbits
Byte	Byte	8 bits
KiloByte(KB)	KibiByte (KiB)	1024 Bytes
MegaByte(MB)	MebiByte (MiB)	1024 KB
GigaByte(GB)	Gibibyte (GiB)	1024 MB
TeraByte(TB)	Tebibyte (TiB)	1024 GB
PetaByte(PB)	Pebibyte (PiB)	1024 TB
HexaByte or exaByte (EB)	Exbibyte (EiB)	1024 PB
ZettaByte (ZB)	Zebibyte (ZiB)	1024 EB
YottaByte (YB)	Yobiibyte (YiB)	1024 ZB

1.4 Digital systems

Digital systems are designed to store and process and exchange information in digital form. They are found in a wide range of applications, including process control, communication systems, digital instruments, and consumer products. These systems/circuits may be classified by the number of *appropriate* loops enclosed within [4]; more loops will mean more autonomy, therefore *smarter* circuits.

0 - loop circuits: contain only combinational circuits (logic gates)

1 - loop circuits: the memory circuits, with behavioral autonomy in their own internal states; they are mainly used for *storing*

2 - loops circuits: the automata, with the behavioral autonomy in their own state space, performing mainly the function of *sequencing*

3 - loops circuits: the processors, with the autonomy in interpreting their own internal states; they perform the function of *controlling*

4 - loops circuits: the computers, which interpret autonomously the programs according to the internal *data*

n-loop circuits: systems in which the information is interpenetrated with the physical structures involved in processing it; the distinction between *data* and *programs* is surpassed and the main novelty is the *self-organizing* behavior.

Any k-loop circuit can do everything any k-1 loop circuit can do.

While 0 – loop circuits (combinational logic circuits) are quite easy to grasp as they are very simple in structure and behavior, the more evolved circuits, containing sequential circuits (with the clock signal driving them) are the ones used to handle complexity.

Some common 0-loop circuits are: logic gates, multiplexers (sends the selected digital input to the output), demultiplexers (send the input to the selected output), decoders (sends logic 1 to the selected output), adders, subtractors, ALUs (arithmetical-logical units), equality comparators, magnitude comparators etc.

Some common sequential circuits are flip-flops (FFs), registers, counters/timers, and FSMs.

1.5 The advantages of using digital systems

The world is analog, therefore, interacting with it, using digital systems, implies conversion between analog to digital and back.

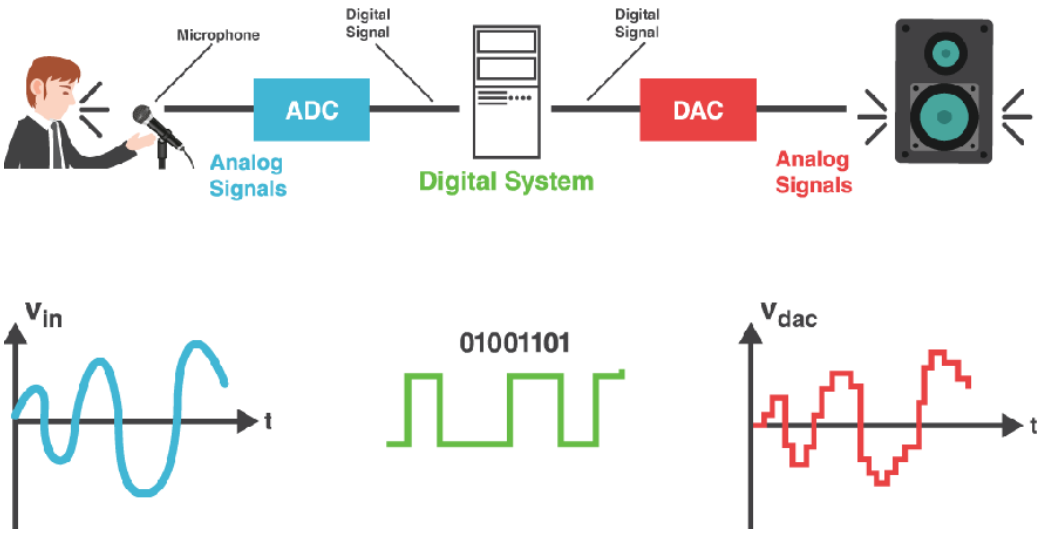


Figure 4. Analog to digital conversion, digital processing and digital to analog conversion example

The main advantages of using a digital system:

- Error correction: math (using numbers) can help a lot to find errors and correct them
- Noise tolerance: copy of a copy may be digitally identical, whereas copy of a copy in analog storage is never the same. Keeping numbers in base2, allows maximum noise immunity as the digital system only has to discriminate between the two possible different symbols. In analog,
- Compression: crunching numbers is possible when
- Modularity: data transfers between digital modules, imply that data processing in a digital system is modular, therefore, there is a high chance of reusability in both hardware modules and software modules. Modular is good as it allows divide-et-impera method of problem-solving.
- Encryption: it is easy to scramble and obfuscate data in other data
- Repeaters: low-cost repeaters and they only have to amplify two symbols accurately (the noise of the repeater can be high)
- Compromise of space & compute power: it can be done in the field, not in the factory. Digital systems are easily configurable to save space and power with acceptable compromises on quality

2. The FPGA (Field Programmable Gate Array)

The FPGA is an semiconductor device based on a matrix of reconfigurable logic blocks (CLBs) as seen in Figure 5. The advantage of this device is that it can be reconfigured to emulate any digital circuit of a certain complexity, in the field (not in the factory!). The interconnection can relay signals coming from any direction to signals going towards any direction. The I/O cells allow signals to travel between the FPGA and outer world.

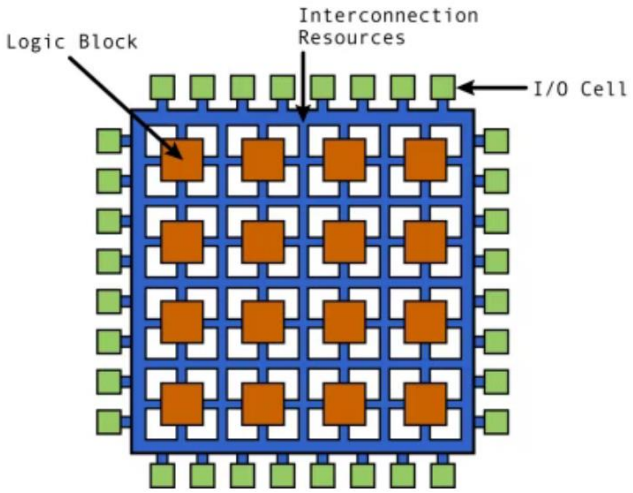


Figure 5. Generic FPGA Architecture Overview

An example of a configurable logic block (CLB) is exemplified below, in Figure 6.

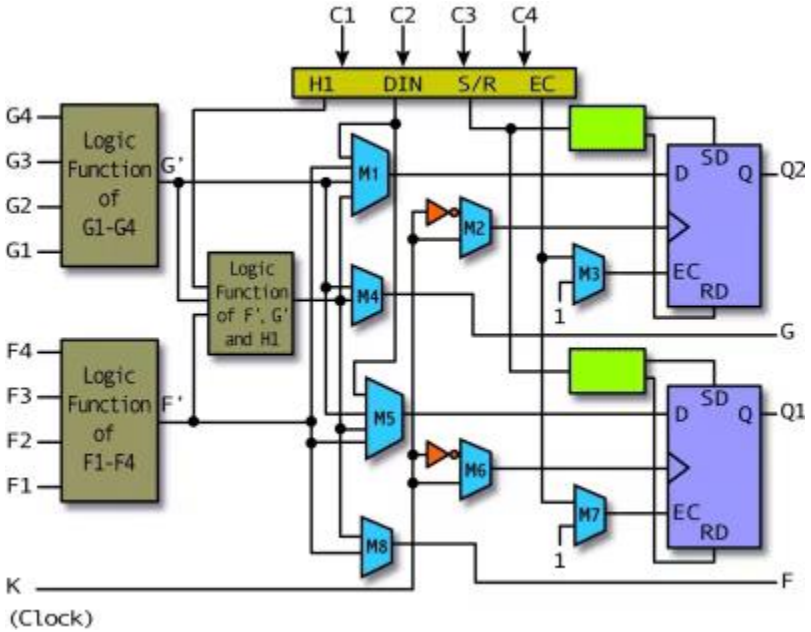


Figure 6. Xilinx CLB. Blue blocks are multiplexers, violet blocks are FFs and dark-green blocks are LUTs (look-up tables)

The software tools first convert code into RTL (register-transfer level, a design abstraction which models the synchronous circuit into flow of digital signals between registers and the logical operations performed on them), then from RTL into gates (during synthesis), and then it infers what resources of the FPGA should it use and how to link them in the physical FPGA device (during implementation). The implementation step is where it matters what specific FPGA chip will be used.

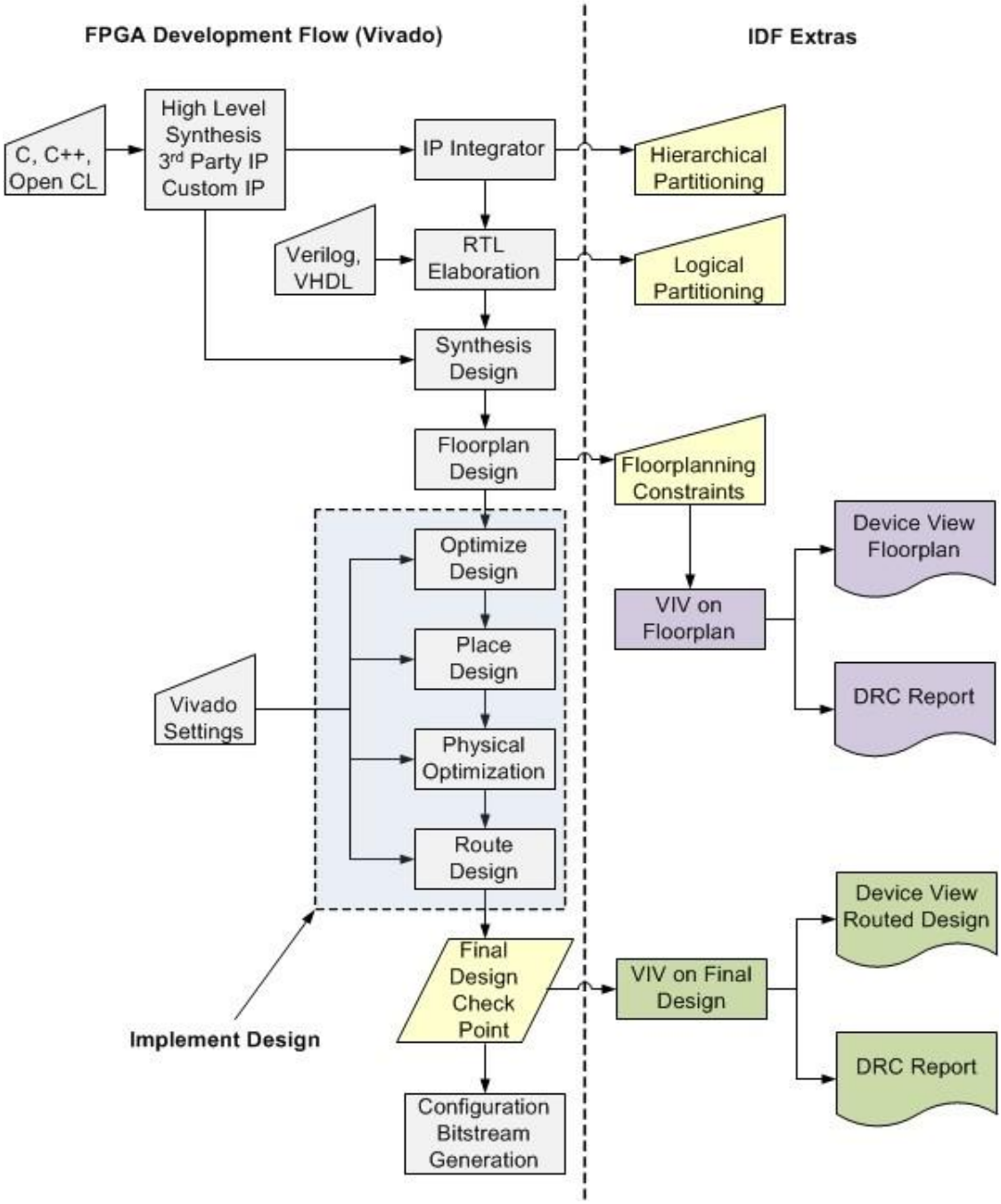


Figure 7. FPGA development flow

Below, there is an FPGA board we will use further, to exemplify digital circuits.

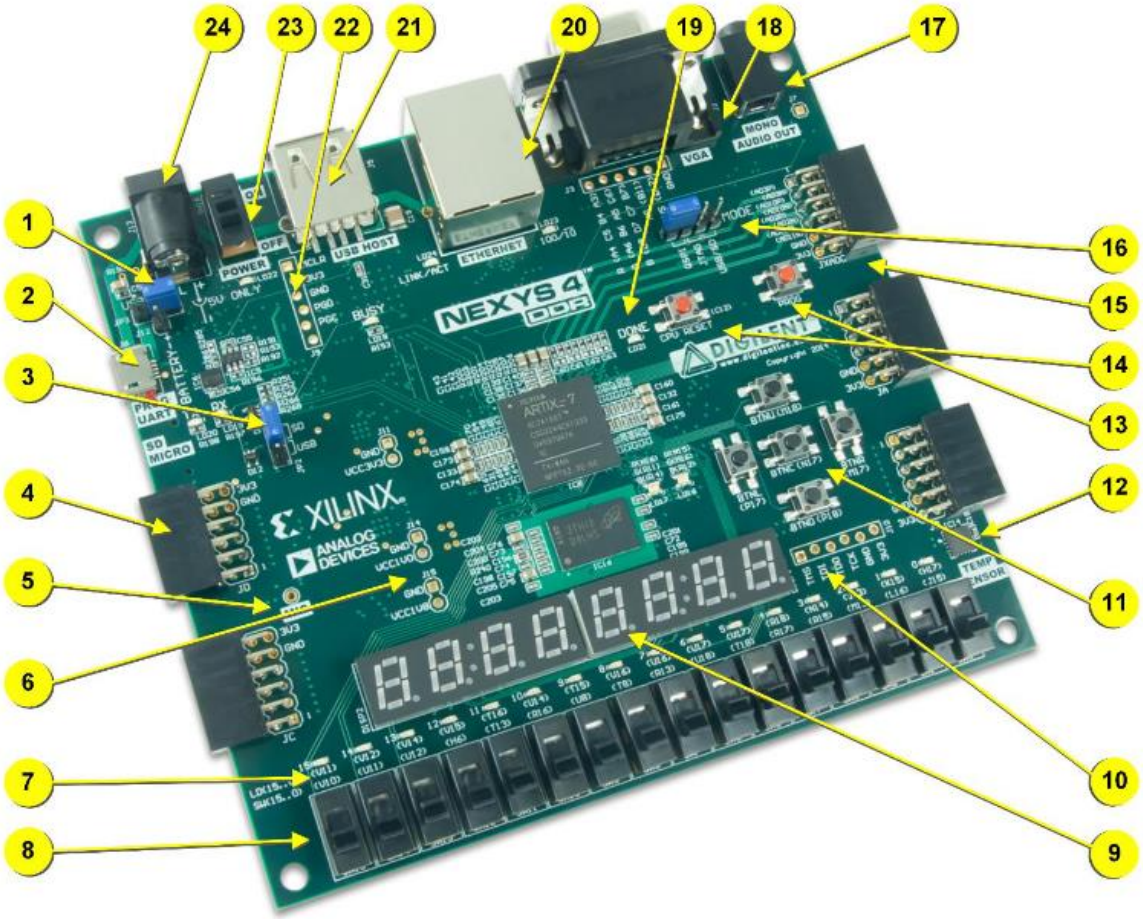


Figure 8. The Nexys 4 DDR FPGA board

Callout	Component Description	Callout	Component Description
1	Power select jumper and battery header	13	FPGA configuration reset button
2	Shared UART/ JTAG USB port	14	CPU reset button (for soft cores)
3	External configuration jumper (SD / USB)	15	Analog signal Pmod port (XADC)
4	Pmod port(s)	16	Programming mode jumper
5	Microphone	17	Audio connector
6	Power supply test point(s)	18	VGA connector
7	LEDs (16)	19	FPGA programming done LED
8	Slide switches	20	Ethernet connector
9	Eight digit 7-seg display	21	USB host connector
10	JTAG port for (optional) external cable	22	PIC24 programming port (factory use)
11	Five pushbuttons	23	Power switch
12	Temperature sensor	24	Power jack

Figure 9. Nexys 4 DDR board features

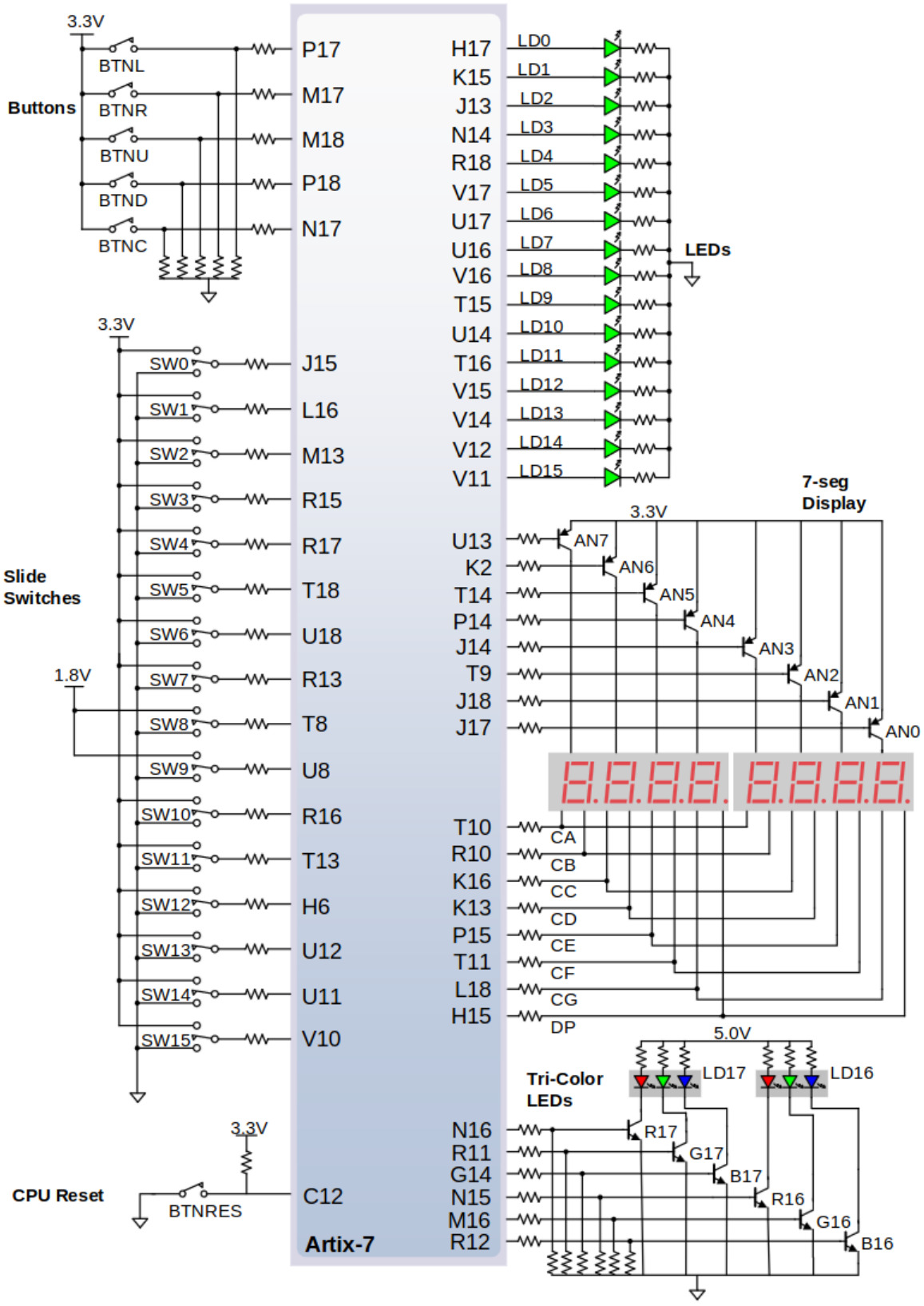


Figure 10. GPIO devices on the Nexys4 DDR FPGA board

2. Zero-loop systems

2.1 Prerequisites

2.1.1 Binary and Boolean Logic

Boolean algebra is a branch of algebra, where the values of the variables are truth values (true and false) usually coded as 1 and 0 and uses logical operators such as AND (conjunction), OR (disjunction), NOT (negation). It was introduced by English mathematician George Boole in the book "The Mathematical Analysis of Logic" in 1847.

A logical operation is a function of two variables and may be expressed using a truth table as below:

Table 2. A (general) logic operation's truth table

A	B	OP (A, B)
FALSE	FALSE	?
FALSE	TRUE	??
TRUE	FALSE	???
TRUE	TRUE	????

There are 16 dual-input single-output logical operations, 3 of which are most used (hence named). The 16 number comes from the output: there are 4 bits of 0 or 1 (one for every combination of A and B), therefore, there are 16 different output configurations => 16 different gates. Their truth table is as below:

Table 3. Truth tables for AND, OR and NOT operations

A	B	A and B	A or B	Not A
FALSE	FALSE	FALSE	FALSE	TRUE
FALSE	TRUE	FALSE	TRUE	TRUE
TRUE	FALSE	FALSE	TRUE	FALSE
TRUE	TRUE	TRUE	TRUE	FALSE

Table 4. Truth tables for AND, OR and NOT operations (seen as 1-bit operations)

A	B	A and B	A or B	Not A
0	0	0	0	1
0	1	0	1	1
1	0	0	1	0
1	1	1	1	0

2.1.2 Digital Gates

The electronic circuits used to implement Boolean logic are the logical gates. Nowadays, all gates are made of transistors (a semiconductor device used to amplify or switch electrical signals and power). For example, the NOT gate is made of two CMOS transistors (a p-channel and n-channel MOS transistor), as seen in Figure 4 below.

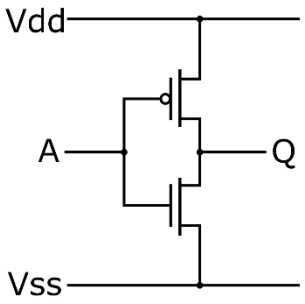


Figure 11. NOT gate ("inverter") made of one pMOS (top) and one nMOS (bottom) transistor.

Vdd is usually at least 1.8V over Vss, and Vss is usually ground. When A is "low," pMOS transistor conducts current and draws Q close to Vdd ("high") whereas nMOS is not conducting. When A is "high" level, nMOS conducts and ties Q to the Vss level ("low").

Engineers use the symbols of such gates, in logic schematics; these symbols, are ratified by international standards as seen in Figure 5.

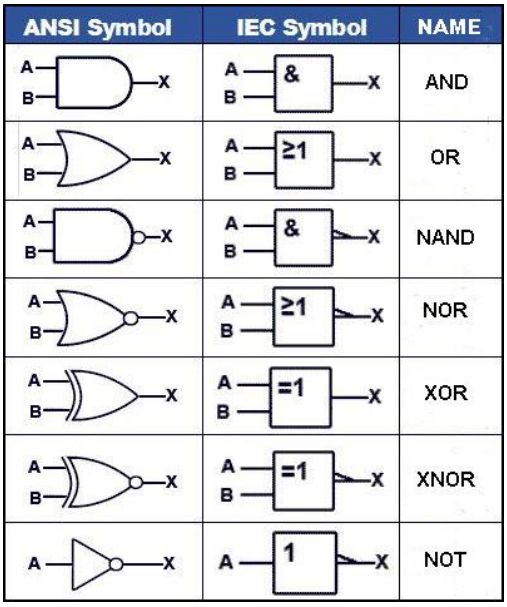
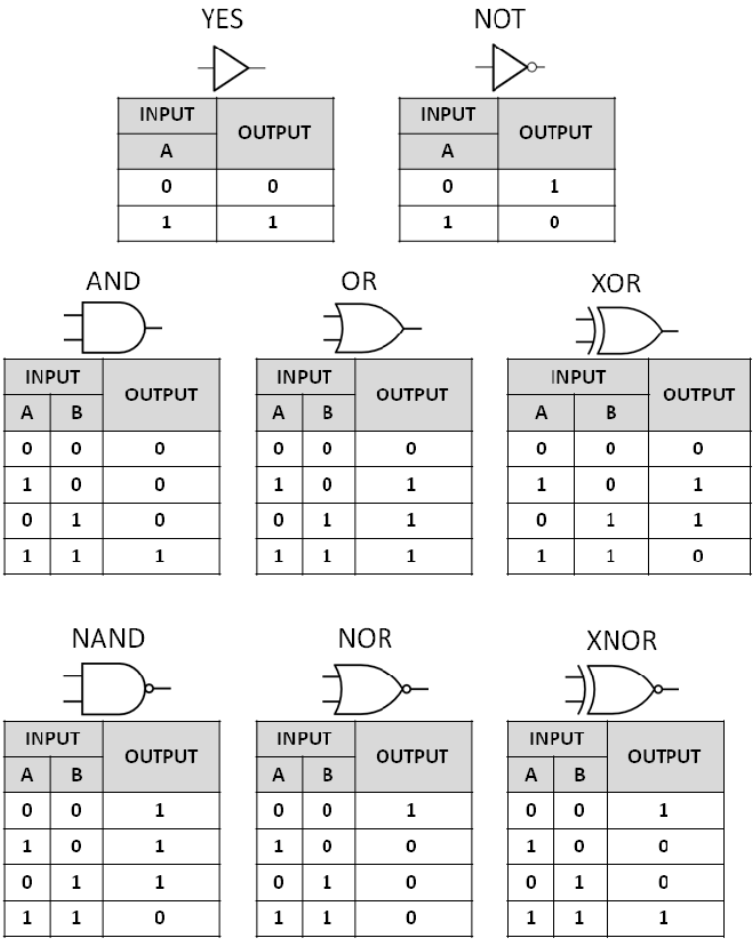


Figure 12. ANSI / IEC [5] (right) and MIL-STD-806B [6] (left) symbols foremost common 7/16 dual-input logic gates (elementary), with their names.



YES

INPUT A	OUTPUT
0	0
1	1

NOT

INPUT A	OUTPUT
0	1
1	0

AND

INPUT A	INPUT B	OUTPUT
0	0	0
1	0	0
0	1	0
1	1	1

OR

INPUT A	INPUT B	OUTPUT
0	0	0
1	0	1
0	1	1
1	1	1

XOR

INPUT A	INPUT B	OUTPUT
0	0	0
1	0	1
0	1	1
1	1	0

NAND

INPUT A	INPUT B	OUTPUT
0	0	1
1	0	1
0	1	1
1	1	0

NOR

INPUT A	INPUT B	OUTPUT
0	0	1
1	0	0
0	1	0
1	1	0

XNOR

INPUT A	INPUT B	OUTPUT
0	0	1
1	0	0
0	1	0
1	1	1

Figure 13. The truth tables for the most commonly used logic gates.

All the 2-input gates are called elementary (or basic) gates. Similarly, for all circuits that are expressed in a iterative or recursive way, the very first instance is called “elementary”.

2.1.3 Complexity in digital circuits

A complex circuit is a circuit that has spatial complexity (structure) or behavior complexity or a combination of the two.

To express spatial complexity, two metrics are used:

- the SIZE (S) of the circuit (the number of elementary gates)
- the DEPTH (D) of the circuit (the largest number of elementary gates passed through, when the signal goes from any input to any output)

An elementary gate (2-input, 1-output) has the S = 1 and D = 1.

2.1.4 Complexity classes

A more in-depth talk on complexity for algorithms may be found in [491], below is an extract of how complexity applies to circuits. Complexity is usually expressed as Big-O notation. The complexity of a function f is decided by finding another function g, which asymptotically bounds the f function.

Mathematically, this is expressed as: if f(n) has the same complexity as g(n), then from n = k onwards, the c*g(n) >= f(n), where k is a point < infinity and c is a constant

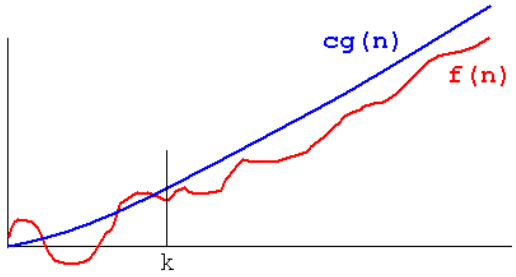


Figure 14. Representing a g(n) function which asymptotically bound f(n) function.

To learn more about Big-Oh, Big-Theta and Big-Omega and their small variants, see [99]. A list of common complexity classes is listed below. O(1) means constant time, and is the best one can hope for: the algorithm runtime will not increase with data increase, the circuit will not increase its size no matter the number of inputs etc.

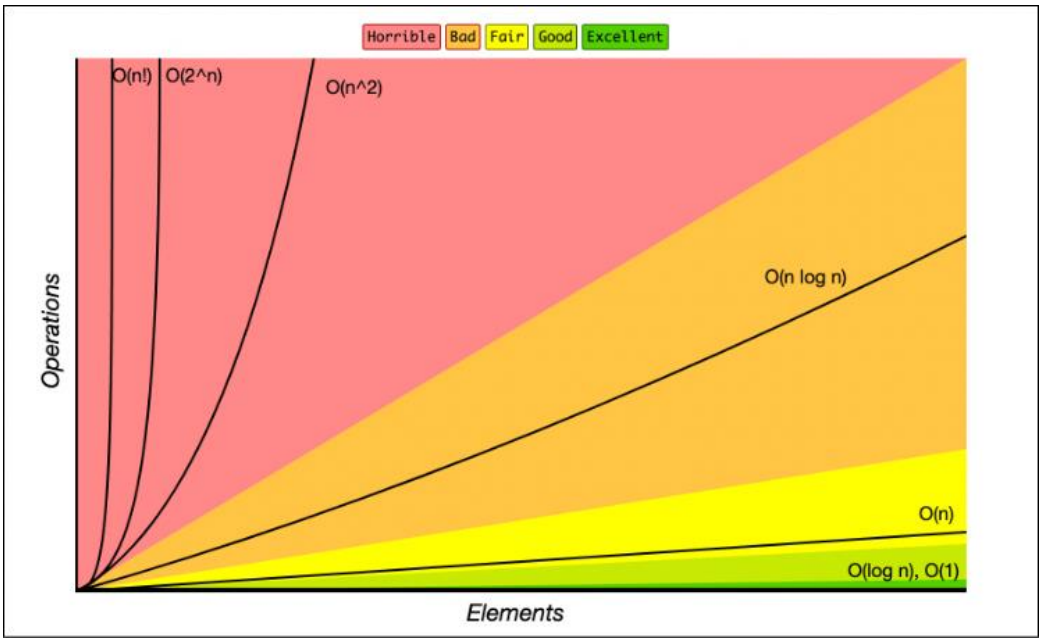


*Figure 15. The O-notation complexity increases with the number of elements processed. O(1) and O(logn) are usually excellent complexities, O(n) is fair, and O(n*logn) is usually considered almost decent in algorithms and circuits*

To better understand the complexity difference between O(logN) and O(N) we propose the next game: one thinks at a number from 0 to 100. Assuming another one tries to guess the number, with hints of “my number is higher” or “my number is lower”:

- in O(N) algorithm (brute forcing all values) one will guess in at most 100 steps
- whereas in O(logN) algorithm, same task will take at most 7 steps (assuming log2).

This is not very impressive, but as one goes further (towards infinity), the advantage will become obvious. Assume the same game, but with numbers from 0 to 4 billion:

- in O(N) algorithm it will take at most 4 billion steps
- whereas in O(logN) it will take at most 32 steps!

This is the power of the logarithm: it goes to infinity with N going to infinity, but much slower.

To better understand how this applies to circuits, imagine an N-input AND gate, implemented with N-1 elementary gates, arranged in logN layers as below:

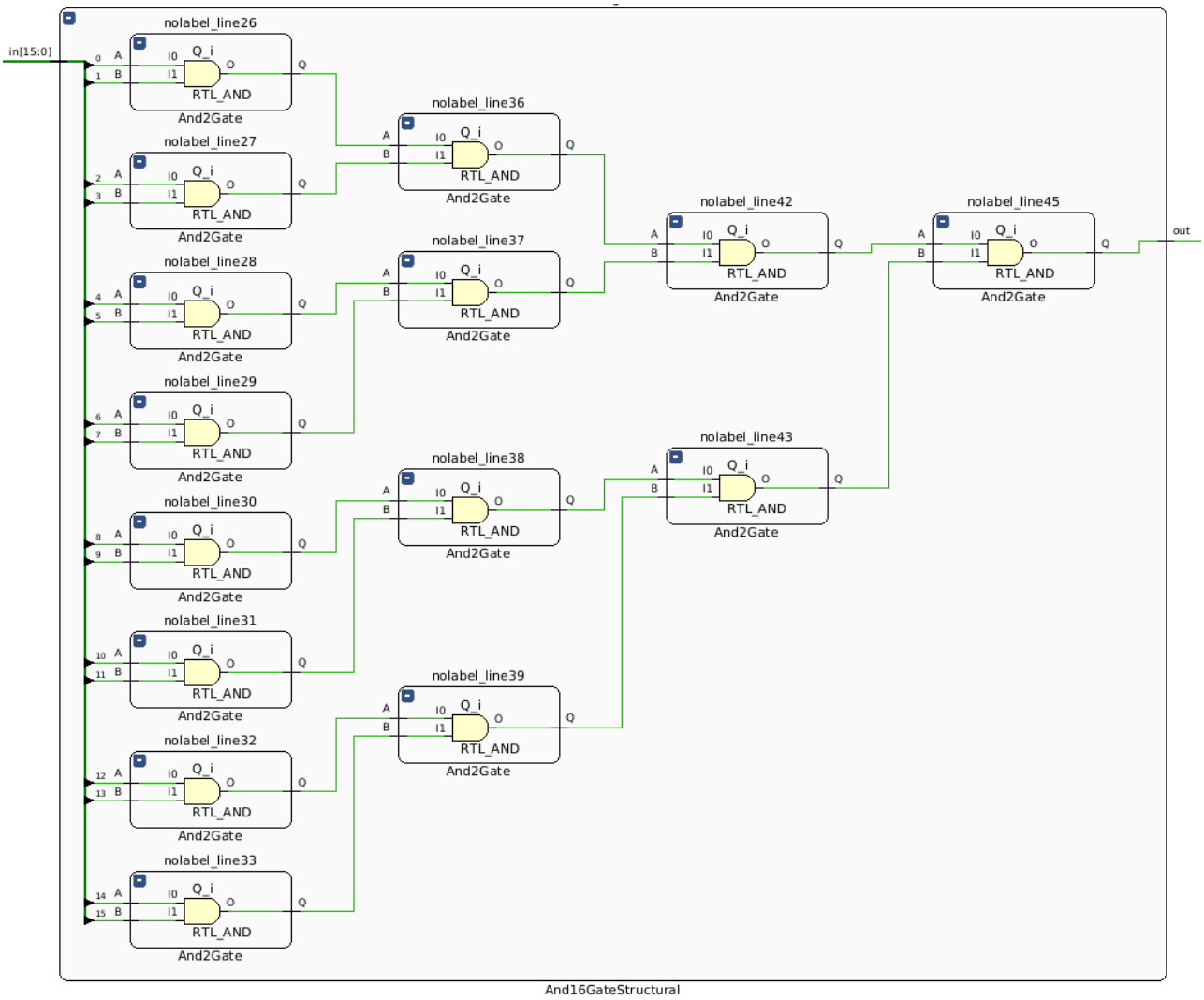


Figure 16. A 16-input AND gate built from 2-input AND gates.

2.1.4 Verilog syntax

S. Winberg and J. Taylor [8] summarized the most important syntax features of Verilog language in their cheat sheet:

Comments

```
// One-liner
/* Multiple
   lines */
```

Numeric Constants

```
// The 8-bit decimal number 106:
8'b_0110_1010 // Binary
8'o_152       // Octal
8'd_106       // Decimal
8'h_6A        // Hexadecimal
"j"           // ASCII

78'bZ          // 78-bit high-impedance
```

Too short constants are padded with zeros on the left. Too long constants are truncated from the left.

Nets and Variables

```
wire [3:0]w; // Assign outside always blocks
reg  [1:7]r; // Assign inside always blocks
reg  [7:0]mem[31:0];

integer j; // Compile-time variable
genvar  k; // Generate variable
```

Parameters

```
parameter  N     = 8;
localparam State = 2'd3;
```

Assignments

```
assign Output = A * B;
assign {C, D} = {D[5:2], C[1:9], E};
```

Operators

```
// These are in order of precedence...
// Select
A[N] A[N:M]
// Reduction
&A ~&A |A ~|A ^A ~^A
// Compliment
!A ~A
// Unary
+A -A
// Concatenate
{A, ..., B}
// Replicate
{N{A}}
// Arithmetic
A*B A/B A%B
A+B A-B
// Shift
A<<B A>>B
// Relational
A>B A<B A>=B A<=B
A==B A!=B
// Bit-wise
A&B
A^B A~^B
A|B
// Logical
A&&B
A||B
// Conditional
A ? B : C
```

Module

```
module MyModule
#(parameter N = 8) // Optional parameter
 (input  Reset, Clk,
  output [N-1:0]Output);
 // Module implementation
endmodule
```

Module Instantiation

```
// Override default parameter: setting N = 13
MyModule #(13) MyModule1(Reset, Clk, Result);
```

Figure 17. Verilog syntax cheat sheet (1/2)

Case

```
always @(*) begin
 case(Mux)
  2'd0: A = 8'd9;
  2'd1,
  2'd3: A = 8'd103;
  2'd2: A = 8'd2;
  default:;
 endcase
end

always @(*) begin
 casex(Decoded)
  4'b1xxx: Encoded = 2'd0;
  4'b01xx: Encoded = 2'd1;
  4'b001x: Encoded = 2'd2;
  4'b0001: Encoded = 2'd3;
  default: Encoded = 2'd0;
 endcase
end
```

Synchronous

```
always @(posedge Clk) begin
 if(Reset) B <= 0;
 else      B <= B + 1'b1;
end
```

Loop

```
always @(*) begin
 Count = 0;
 for(j = 0; j < 8; j = j+1)
  Count = Count + Input[j];
end
```

Function

```
function [6:0]F;
 input [3:0]A;
 input [2:0]B;
 begin
  F = {A+1'b1, B+2'd2};
 end
endfunction
```

Generate

```
genvar j;
wire [12:0]Output[19:0];

generate
 for(j = 0; j < 20; j = j+1)
 begin: Gen_Modules
  MyModule #(13) MyModule_Instance(
   Reset, Clk,
   Output[j]
  );
 end
endgenerate
```

State Machine

```
reg   [1:0]State;
localparam Start = 2'b00;
localparam Idle  = 2'b01;
localparam Work  = 2'b11;
localparam Done  = 2'b10;

reg tReset;

always @(posedge Clk) begin
 tReset <= Reset;

 if(tReset) begin
  State <= Start;

 end else begin
  case(State)
   Start: begin
    State <= Idle;
   end
   Idle: begin
    State <= Work;
   end
   Work: begin
    State <= Done;
   end
   Done: begin
    State <= Idle;
   end
   default:;
  endcase
 end
end
```

Figure 18. Verilog syntax cheat sheet (2/2)

2.1.5 VHDL syntax

GRAY_ITALICS represent user-defined names or operations — keywords
Purple constructs are only available in VHDL 2008. — literals (constants)

```
-- This is a comment
/* Multi-line comment
   (VHDL 2008 only) */
library IEEE;
use IEEE.std_logic_1164.all;
use IEEE.numeric_std.all;
```

You almost always need these libraries; just put this at the top of every file.

```
entity ENTITY_NAME is
  port(
    PORT_NAME : in std_logic; -- Single bit input
    ANOTHER   : out std_logic_vector(3 downto 0) -- 4-bit output
    );
end;
```

No semicolon on the last one!

Don't forget these semicolons!

```
architecture ARCH_NAME of ENTITY_NAME is
  -- Component declarations, if using submodules
  component SUB_ENTITY is
    port(
      -- Port list for the entity you're including
    );
  end component;

  -- Signal declarations, if using intermediate signals
  signal NAME : TYPE;
begin
  -- Architecture definition goes here
end;
```

Just replace `entity` with `component` and put `end component` at the end.

Instantiate a submodule

```
INSTANCE_NAME : MODULE_NAME
    generic map (
        GENERIC => CONSTANT,
    )
    port map(
        PORT => VALUE,
        ANOTHER => LOCAL_SIGNAL
    );
```

Continuous assignments

```
RESULT_SIGNAL <= SIGNAL1 and SIGNAL2;
```
Also works for or, not, nand, nor, xor

```
RESULT_SIGNAL <= '1' when (SIGNAL1 = x"5") else '0';
```
Note '=' for comparison (not '==')

```
HIGHEST_BIT <= EIGHT_BIT_VEC(7);
```
Extract a single bit (7 is MSB, 0 is LSB)

```
TWO_BIT_VEC <= EIGHT_BIT_VEC(3 downto 2);
```
Extract multiple bits

```
SIX_BIT_VEC <= "000" & EIGHT_BIT_VEC(3 downto 2) & SINGLE_BYTE;
```
Concatenate

Types

`std_logic` Basic logic type, can take values 0, 1, X, Z (and others)

`std_logic_vector (n downto m)` Ordered group of std_logic

`unsigned (n downto m)`
`signed (n downto m)`
Like std_logic_vector, but preferred for numerically meaningful signals

`integer` Poor for synthesis, but constants are integers by default

Literals

`'0', '1', 'X', 'Z'`

`"00001010", x"0c"` 8-bit binary, hex

`9x"101"` 9-bit hex — `3b"101"` 3-bit binary — `7d"101"` 7-bit decimal

`5, 38, 10000000`

Type conversion

`to_unsigned(INTEGER, WIDTH)` Use `to_unsigned` for unsigned constants before VHDL 2008.

`unsigned(LOGIC_VECTOR)` (Same things for signed)

`std_logic_vector(UNSIGNED)`

Figure 19. VHDL cheat sheet (1/2)

Process blocks

```
process (SENSITIVITY) is
begin
  -- if/case/print go here
end process;
```

If sensitivity includes:

- `all↕` → Combinational logic
- `clk↑` → Flip-flop / register
- `clk↑ + data↕` → Latch
- Nothing → Testbench (repeated evaluation)
- Something else → Bad things you probably didn't want

Specify all signals by name prior to VHDL 2008

Reporting stuff

```
assert CONDITION report "MESSAGE" severity error;
```
Print message if condition is false

```
report "MESSAGE" severity error;
```
Severity can be NOTE, WARNING, ERROR, FATAL
"FATAL" ends the simulation

```
report "A is " & to_string(a);
```
Use `image` function prior to VHDL 2008

```
report "A in hex is " & to_hstring(a);
```
concatenation; conversion to string

Writing to files (or stdout)

```
variable BUF : line;
```
Declare buffer in process block

```
write(BUF, string'("MESSAGE"));
```
Append message to buffer

```
writeline(output, BUF);
```
Write buffer to stdout (like `report`, but just the text)

```
file RESULTS : text;
```
Declare file handle in process block

```
file_open(RESULTS, "FILENAME", WRITE_MODE);
writeline(RESULTS, BUF);
```

If/else

```
if CONDITION then
  SIGNAL <= VALUE1;
elsif OTHER_CONDITION then
  SIGNAL <= VALUE2;
else
  SIGNAL <= VALUE3;
end if;
```

Note spelling of "elsif"!

Sequential logic

```
process (CLOCK) is
begin
  if rising_edge(CLOCK) then
    -- Clocked assignments go here
  end if;
end process;
```

Case

```
case INPUT_SIGNAL is
  when VALUE1 => OPERATION1;
  when VALUE2 => OPERATION2;
  when others => DEFAULT;
end case;
```

For loop

```
for INDEXVAR in MIN to MAX loop
  -- loop body here
end loop;
```

To count down:

```
for INDEXVAR in MAX downto MIN loop
```

Enumerated types

```
type TYPENAME is (VAL1, VAL2, VAL3);
```

```
signal NAME : TYPENAME;
```
Just like any other type

Figure 20. VHDL cheat sheet (2/2)

To express the AND gate behavior in Figure 21 one has to write in Verilog the code or VHDL code below.

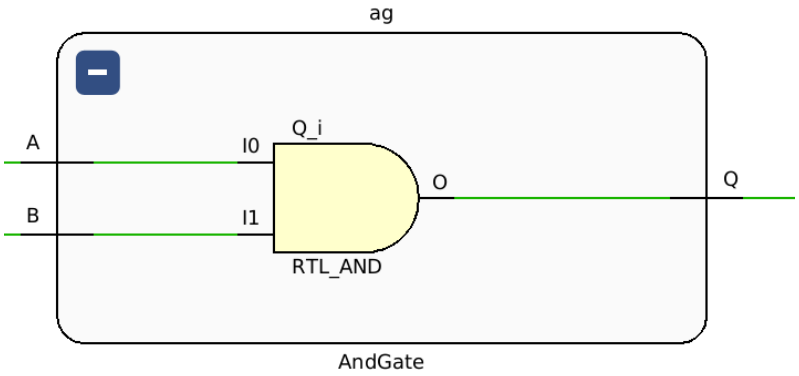


Figure 21. 2-input AND gate

```
module AndGate(input A, input B, output Q);

   assign Q = A & B;

endmodule
```

Figure 22. Verilog code (dataflow) for a 2-input AND gate

```
library IEEE;
use IEEE.std_logic_1164.all;

-- Entity declaration
entity andGate is
   port(A : in std_logic;      -- AND gate input
        B : in std_logic;      -- AND gate input
        Q : out std_logic);    -- AND gate output
end andGate;

-- Dataflow Modelling Style
-- Architecture definition
architecture andLogic of andGate is
 begin
   Q <= A AND B;
end andLogic;
```

Figure 23. Verilog code (dataflow) for a 2-input AND gate

2.4 Theory & Exercises

2.4.1 Multiple-input gates

Using only elementary (2-input) gates, create a 4-input AND gate. Write code in both dataflow and structural manner. Describe the circuit in both in Verilog and VHDL language.

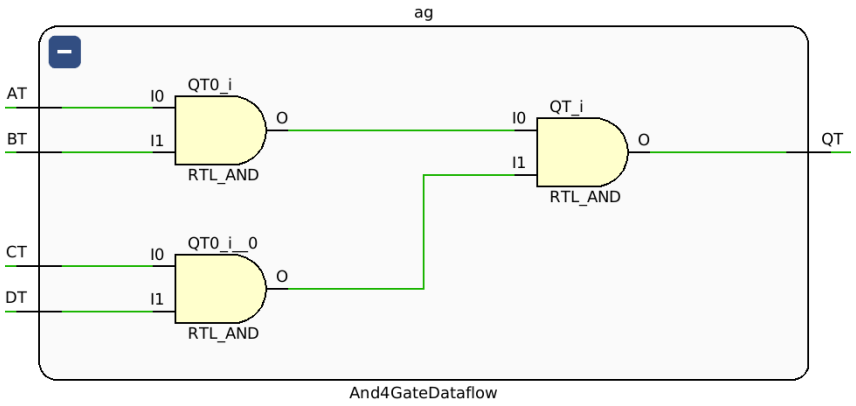


Figure 24. 4-input AND gate from 2-input AND gates (dataflow)

```
module And4GateDataflow(input AT, input BT, input CT, input DT, output QT);
   assign QT = AT & BT & CT & DT;
endmodule
```

Figure 25. Verilog description for 4-input AND (dataflow)

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity And4Gate is
   Port ( AT : in STD_LOGIC;
          BT : in STD_LOGIC;
          CT : in STD_LOGIC;
          DT : in STD_LOGIC;
          QT : out STD_LOGIC);
end And4Gate;

architecture and4Logic of And4Gate is
begin
   QT <= AT AND BT AND CT AND DT;
end and4Logic;
```

Figure 26. VHDL description for 4-input AND (dataflow)

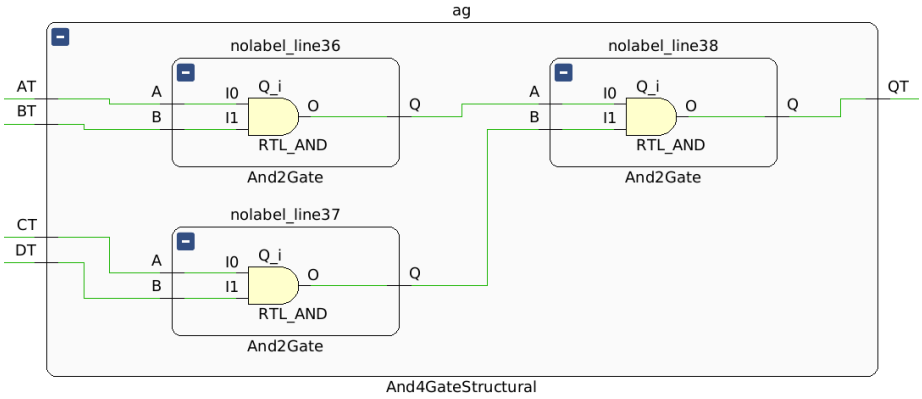


Figure 27. 4-input AND gate from 2-input AND gates (structural)

```
module And2Gate(input A, input B, output Q);
   assign Q = A & B;
endmodule

module And4GateStructural(input AT, input BT, input CT, input DT, output QT);
   wire ABT;
   wire CDT;
   And2Gate(.A(AT), .B(BT), .Q(ABT));
   And2Gate(.A(CT), .B(DT), .Q(CDT));
   And2Gate(.A(ABT), .B(CDT), .Q(QT));
endmodule
```

Figure 28.Verilog description of 4-input AND gate from 2-input AND gates (structural)

A few notes here: assuming N is power of 2, the amount of elementary gates for an N-input AND or OR gate is a having log2 N layers each with half of the number of gates or previous layer. For example, an 16-input AND gate requires 4 layers having the N-1 gates, distributed as follows:

- Layer 1: 8 elementary gates (all 16 inputs go into the inputs of the first layer)
- Layer 2: 4 elementary gates
- Layer 3: 2 elementary gates
- Layer 4: 1 elementary gate (which gives the output of the circuit)

Therefore, the SIZE of the circuit is O(N), and the DEPTH of the circuit is O(logN)

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity And4Gate is
   Port ( AT : in STD_LOGIC;
          BT : in STD_LOGIC;
          CT : in STD_LOGIC;
          DT : in STD_LOGIC;
          QT : out STD_LOGIC);
end And4Gate;

architecture and4LogicStructural of And4Gate is
   component And2Gate
   port(A, B: in std_logic;
          Q: out std_logic);
   end component;
   signal and1_to_and3: std_logic;
   signal and2_to_and3: std_logic;

   begin

   and1: And2Gate port map(AT, BT, and1_to_and3);
   and2: And2Gate port map(CT, DT, and2_to_and3);
   and3: And2Gate port map(and1_to_and3, and2_to_and3, QT);
```

Figure 29. VHDL description of 4-input AND gate from 2-input AND gates (structural)

2.4.2 Elementary multiplexer

A multiplexer is a circuit that outputs one of its inputs, depending on the selection. The elementary multiplexer is draws as follows:

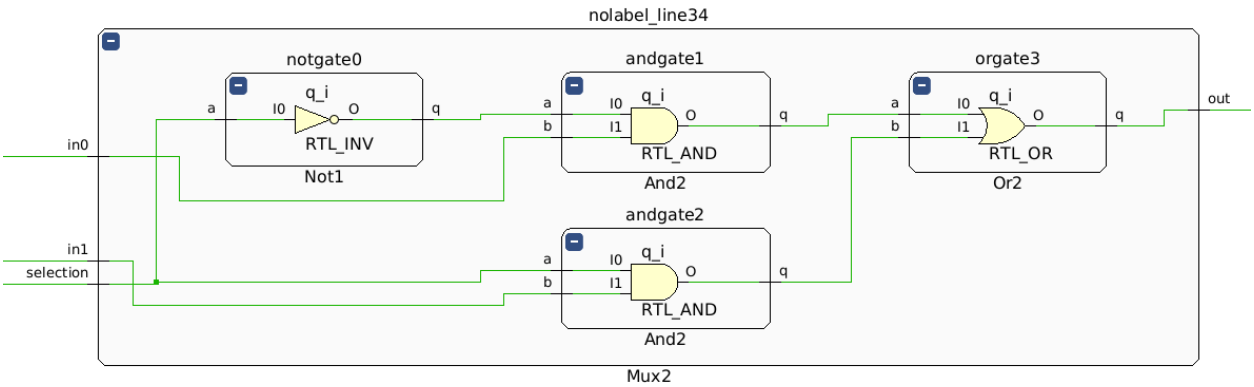


Figure 30. MUX2 implemented with one NOT, two AND, one OR gate(s)

The implementation post-synthesis is done with one LUT, as shown in the

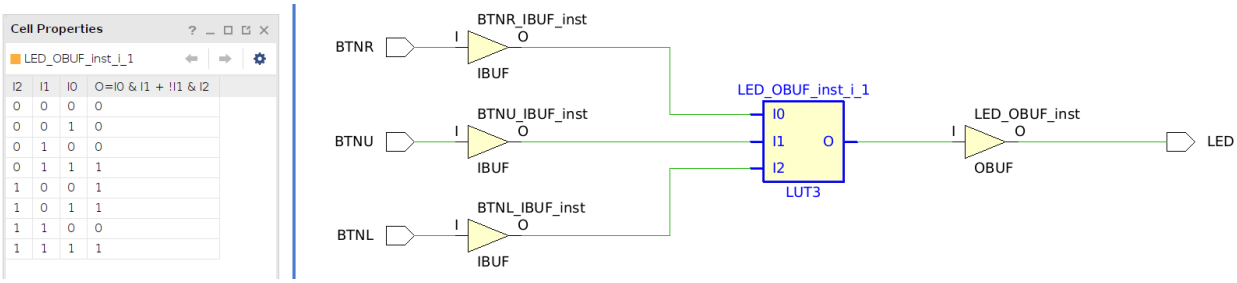


Figure 31. LUT-based implementation of elementary mux, in FPGA

```
module And2(output  q, input a, input b);
   assign q = a & b;
endmodule

module Or2(output  q, input a, input b);
   assign q = a | b;
endmodule

module Not1(output q, input a);
   assign q = ~a;
endmodule

module Mux2(output  out, input selection, input in0, input in1);
   //assign out = (in0*!selection)  | in1*selection;
   //assign out = (selection == 0) ? in0 : in1;

   //structural:
   wire notselection;
   wire w1;
   wire w2;

   Not1 notgate0(.q(notselection),  .a(selection));
   And2 andgate1(.q(w1),  .a(notselection),  .b(in0));
   And2 andgate2(.q(w2),  .a(selection),  .b(in1));
   Or2 orgate3(.q(out),  .a(w1), .b(w2));
```

Figure 32. Verilog description of an elementary MUX

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity Mux2 is
   Port(in0,in1,sel: in STD_LOGIC;
        outp : out STD_LOGIC);
end Mux2;

architecture Mux2a of Mux2 is
   component And2
   port(a,b: in STD_LOGIC;
        q: out STD_LOGIC);
   end component;

   component Or2
   port(a,b: in STD_LOGIC;
        q: out STD_LOGIC);
   end component;

   component Not1
   port(a: in STD_LOGIC;
        q: out STD_LOGIC);
   end component;

   signal w1: STD_LOGIC;
   signal w2: STD_LOGIC;
   signal nsel: STD_LOGIC;

   begin
      andgate1: And2 port map(a => in0, b => nsel, q => w1);
      andgate2: And2 port map(a => in1, b => sel, q => w2);
      notgate3: Not1 port map(a => sel, q => nsel);
      orgate4: Or2 port map(a => w1, b => w2, q => outp);

end Mux2a;
```

Figure 33. VHDL description of an elementary MUX

Exercise: Using elementary MUX (2-input, 1-selection), describe a 4-input MUX. All data is 1-bit wide.

Solution: A hierarchical implementation will be made, with layered MUXes: first layer will have 2x MUXes, and the next layer just 1.

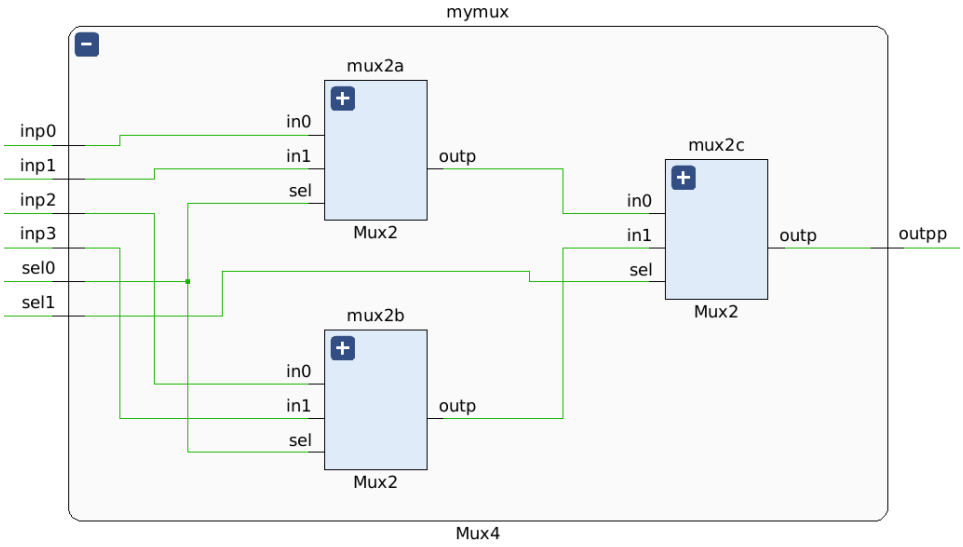


Figure 34. Block schematic for MUX4 made of 3x MUX2

As one may see, the number of layers is $\log_2 N$ => depth is O(logN), and the number of elementary circuits is N-1 => size is O(N).

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity Mux4 is
   Port(inp0, inp1, inp2, inp3: in STD_LOGIC;
      sel0,sel1: in STD_LOGIC;
      outpp : out STD_LOGIC);
end Mux4;

architecture Mux4a of Mux4 is
   component Mux2
   port(in0, in1: in STD_LOGIC;
       sel: in STD_LOGIC;
       outp: out STD_LOGIC);
   end component;

   signal wa: STD_LOGIC;
   signal wb: STD_LOGIC;

   begin
      mux2a: Mux2 port map(in0 => inp0, in1 => inp1, sel => sel0, outp => wa);
      mux2b: Mux2 port map(in0 => inp2, in1 => inp3, sel => sel0, outp => wb);
      mux2c: Mux2 port map(in0 => wa, in1 => wb, sel => sel1, outp => outpp);
```

Figure 35. VHDL description of MUX4 made of MUX2 circuits

Using only elementary …. Describe the circuit in both in Verilog and VHDL language.

3. One-loop systems

Memory unit of 1 bit...

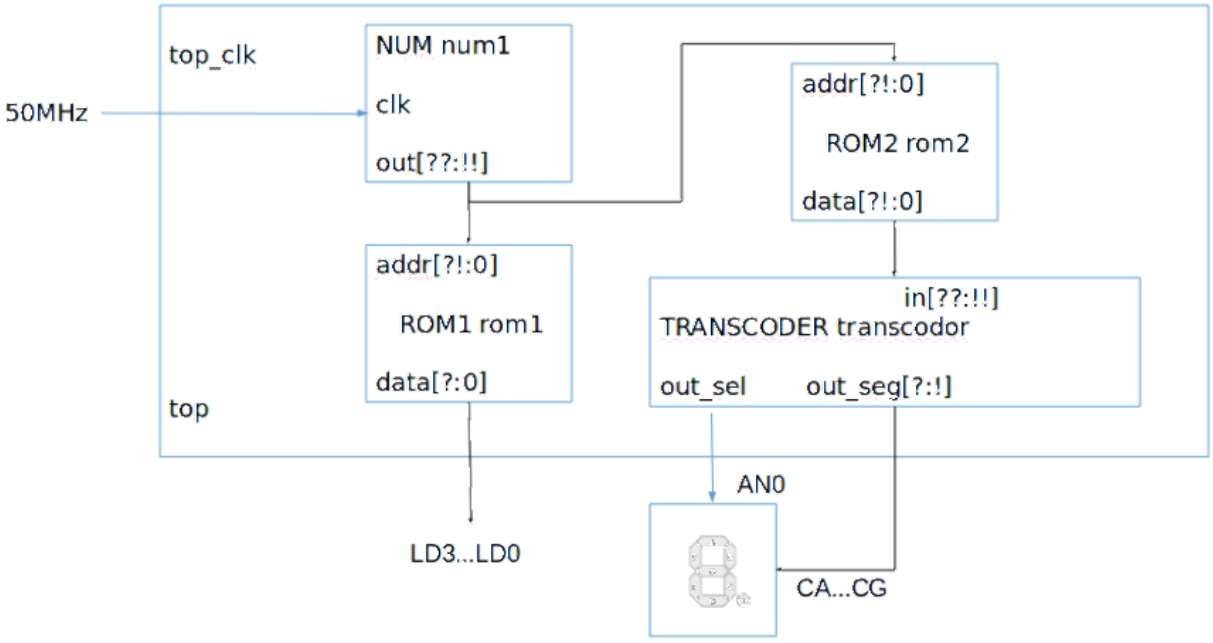
4. Two-loop systems (automata)

4.1 Prerequisites

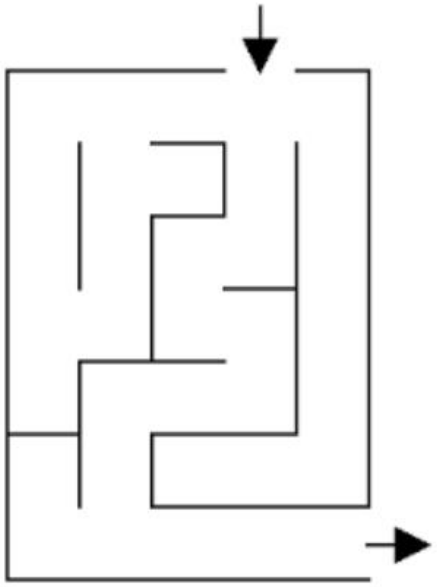
4.2 Theory

4.3 TODO: other exercises

Famous Chip & Dale squirrels want to go to Beautiful Almond Trees. For this, Chip hired you to design and implement an electronic map, for Dale, with the following block schematic:



The map is as follows:



To walk through the maze, the squirrel should go: 3 steps forward, 1 step to the right, 1 step to the left…

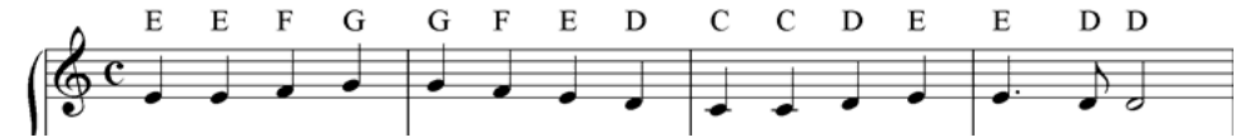
ROM1 memory contains data regarding the direction where the squirrel should go:
1 = Forward, 2 = Backwards, 4 = Left, 8 = Right

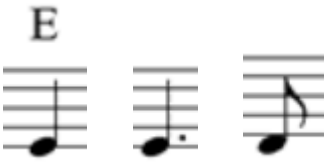
ROM2 memory contains data regarding how many steps the squirrel go in that direction

Iesirea out a numaratorului, isi schimba valoarea la fiecare FIX 1 secunda (veverita isi poate schimba directia doar 1 data pe secunda)

Your task is to write Verilog code for the electronic map.
Punctaj (din 50 de puncte): 6 + 7 + 7 + 4 p, 12p pentru top, 10p pentru "design" si 4p coding style.
Numaratorul de timp NUM (6p):
(1p) numaratorul are dimensiunea minima necesara a registrului de stare interna
(1p) numaratorul are dimensiunea minima necesara a registrului de iesire
(1p) registrul de stare interna se incrementeaza in ritmul corespunzator
(1p) registrul de iesire se incrementeaza in ritmul corespunzator (1 secunda)
(1p) conditia de numarare este corecta
(1p) modulul verilog are denumirea ceruta (NUM)
Memoria de tip ROM1 (7p):
(1p) are numarul minim de adrese / locatii, numele cerut al intrarii
(1p) are numarul minim de biti de iesire, numele cerut al iesirii
(1p) conditia de citire e corecta
(Xp) memoria are continutul corect in proportie de X*25%, (X e maxim 4)
Memoria de tip ROM2 (7p)
(1p) are numarul minim de adrese / locatii, numele cerut al intrarii
(1p) are numarul minim de biti de iesire, numele cerut al iesirii
(1p) conditia de citire e corecta
(Xp) memoria are continutul corect in proportie de X*25%, (X e maxim 4)
Transocodorul de tip TRANSCODER (4p)
(1p) in are dimensiunea, tipul corect, numele cerut
(1p) out_sel are dimensiunea si tipul corect, numele cerut
(2p) out_seg are dimensiunea si tipul corect, numele cerut
top (12p):
(1p) memoria ROM1 este instantiata corect (tip, nume semnale)
(1p) memoria ROM2 este instantiata corect (tip, nume semnale)
(1p) numaratorul este instantiat corect (tip, nume semnale)
(1p) transcodorul este instantiat corect (tip, nume semnale)
(1p) legaturile NUM-ROM1 sunt corecte
(1p) legaturile NUM-ROM2 sunt corecte
(1p) legaturile ROM2-TRANSCODER sunt corecte
(1p) top_clk se leaga corect in modulul de top
(1p) ROM1 se leaga corect in exterior
(1p) TRANSCODER se leaga corect in exterior (top: out_sel)
(2p) TRANSCODER se leaga corect in exterior (top: out_seg)
design (10p):
(3p) design-ul este complet (ca numar / tip de componente) si nu are erori de sintaxa / sinteza / implementare

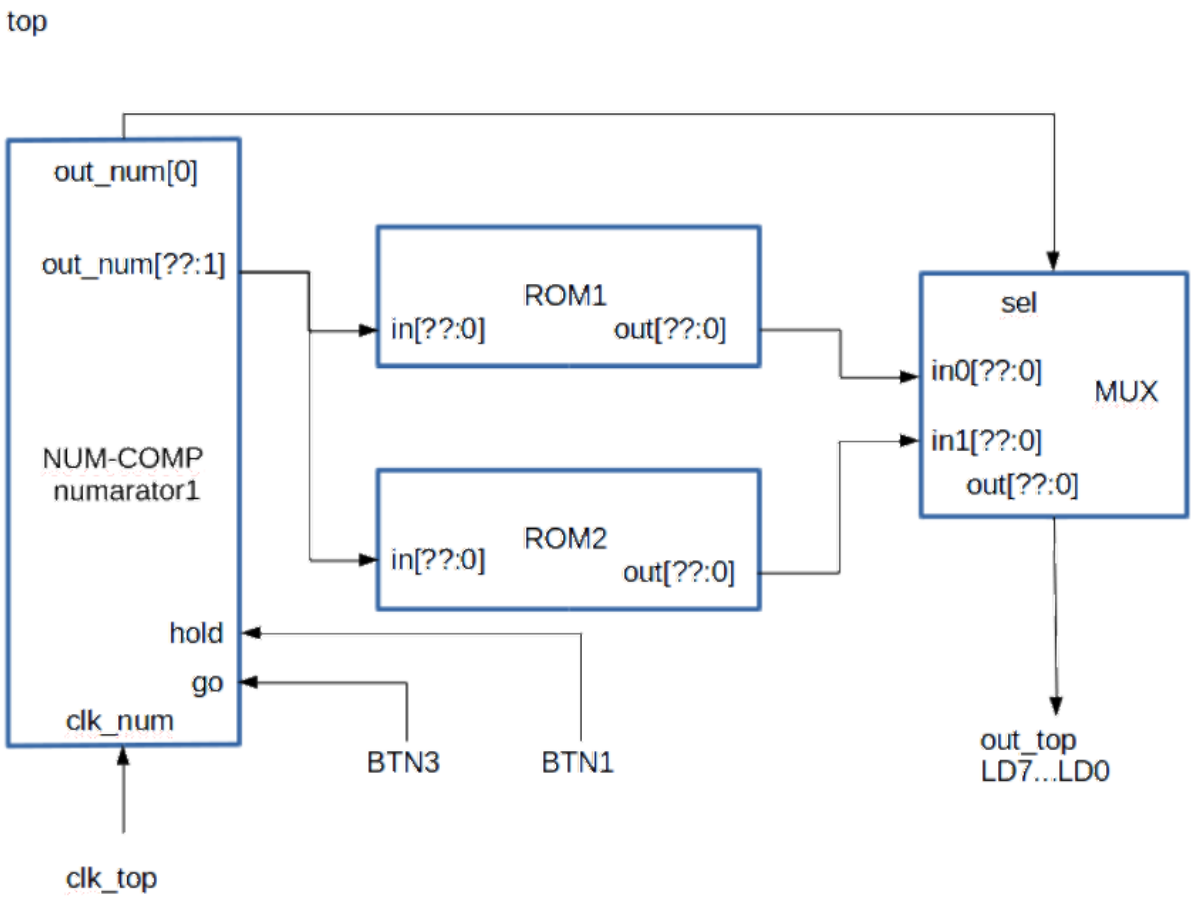
(3p) design-ul functioneaza pe FPGA asa cum s-a cerut (intre stari trec fix. X milisecunde si starile se succed in ordinea ceruta)
(1p) corespondenta semnalului de ceas <> pin e corecta
(1p) corespondenta biti de iesire <> pini e corecta (selectie digit)
(2p) corespondenta biti de iesire <> pini e corecta (segmente)
coding_style(4p): codul este usor de citit (indentat si spatiat similar cu exercitiul din laborator5)





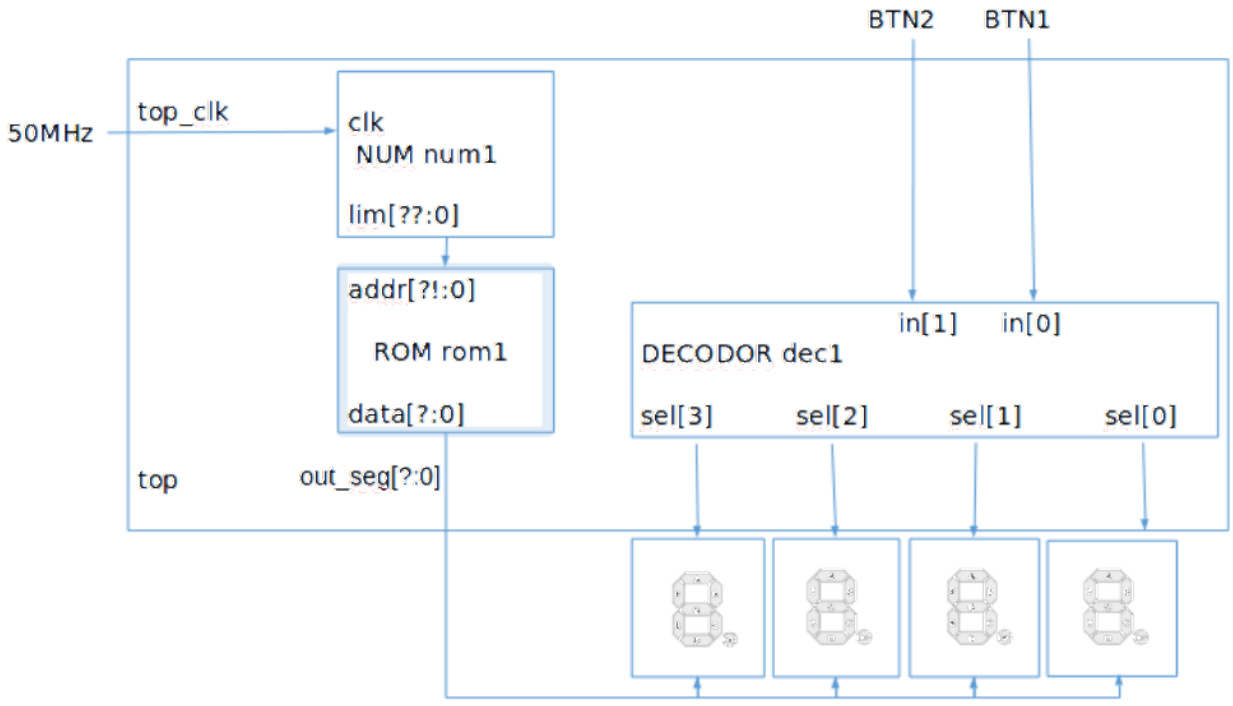
Timp de efectiv de lucru: 50 de minute. SUBIECT_5_FARA_RAM
Extraterestrii din sistemul solar luminat de Betelgeuse, au fost de acord sa ne imprumute un generator ZPM. Drept multumire, oamenii au decis sa tina o serata pentru a le delecta “ochiurechea” (ochiurechea este un organ de simt al extraterestrilor, care transforma impulsurile luminoase in semnale electrice interpretate de creierul lor ca “sunete”)
Este minisunea ta, sa reproduci o parte din Simfonia a 9-a pentru ochiurechile extraterestrilor. La sfarsitul melodiei, se poate introduce o pauza (niciun led aprins) convenabil de lunga apoi se repeta melodia.
Obs1.
• pentru a produce sunetul A, trebuie aprins LD0
• penrtu a produce sunetul B, trebuie aprins LD0 si LD1
• pentru a produce sunetul C, trebuie aprins LD0, LD1, LD2
• pentru a produce sunetul D, trebuie aprinse LD0, LD1, LD2, LD3
• si tot asa.
Obs2. Durata notelor se considera:
• "2 T" pentru notele care arata ca prima nota E (cea mai din stanga)
• "3 T" pentru nota E cu punct (ultima nota E)
• "1 T" pentru notele care arata ca penultima nota D
• "4 T" pentru notele care arata ca ultima nota D (cea mai din dreapta)
unde 1 T inseamna FIX 1 secunda.
Obs3. Se considera echivalenta o nota de 4 T cu 2 de 2 T sau 4 de 1 T.
Obs4.

Numaratorul NUM-COMP:
• contine doua registre:
◦ unul pentru starea interna (care se incrementeaza la fiecare perioada de ceas)
◦ unul pentru iesire "out_num" (care se incrementeaza cand registrul de stare interna a numarat o secunda)
• la fiecare incrementare a iesirii, registrul de stare interna se duce in 0
• NUM-COMP numara cand "go" este 1
• NUM-COMP isi mentine valoarea cand "hold" este 1 si "go" este 0
"ROM1" este o memorie de tip ROM de dimensiune corespunzatoare (minima)
"ROM2" este o memorie de tip ROM de dimensiune corespunzatoare (minima)
"MUX" este un multiplexor
Ceasul din sistem este ceasul generat de oscilatorul de 50 MHz de pe placa cu FPGA.
Implementati in Verilog modulele din circuitul din figura, RESPECTAND numele semnalelor si ale modulelor / instantelor



Timp de efectiv de lucru: 90 de minute. SUBIECT_3_FARA_RAM
"Predator" vrea sa ajute METROREX sa construiasca o linie metrou pana la Aeroportul "Henri Coanda". In acest scop, vrea sa doneze regiei, un ceas cu timer care la terminarea timpului indicat, spulbera roca dura din drumul liniei de metrou.
Indicatorul de timp de pe ceas afiseaza initial toate segmentele aprinse; el apoi marcheaza trecerea

timpului prin stingerea a cate unuia din segmente aprinse, la fiecare FIX 500 milisecunde
La momentul T=0: 7 segmente aprinse
La momentul T=1: 6 segmente aprinse
La momentul T=2: 5 segmente aprinse
La momentul T=3: 4 segmente aprinse
La momentul T=4: 3 segmente aprinse
La momentul T=5: 2 segmente aprinse
La momentul T=6: 1 segment aprins
La momentul T=7: 0 segmente aprinse
"num1" este un numarator de tip NUM care numara in sus, din 1 in 1.
"rom1" este o memorie de tip ROM de dimensiune minima.
"dec1" este un decodor care produce mereu un singur bit de 0 pe iesire (arata care 1 digit este aprins, restul de 3 fiind stinsi)
Ceasul din sistem este ceasul generat de oscilatorul de 50 MHz de pe placa cu FPGA.
Implementati in Verilog modulele din circuitul din figura, RESPECTAND numele semnalelor si ale modulelor / instantelor



Punctaj (din 50 de puncte): 6 + 9 + 3 + 12p pentru top, 16p pentru "design" si 4p coding style.
Detaliu punctaj:
numarator1 (6p):
(1p) numaratorul are dimensiunea minima necesara
(1p) iesirea numaratorului are dimensiunea corecta

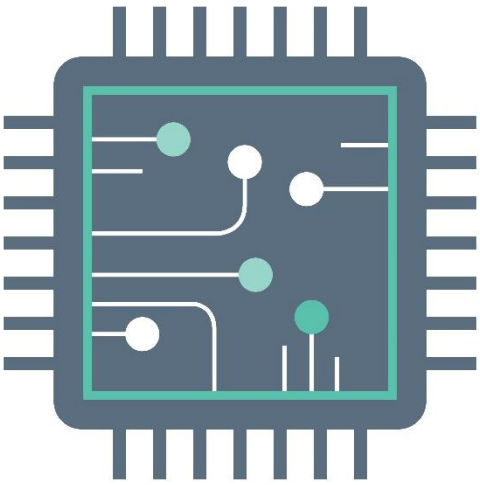
(3p) iesirea numaratorului se schimba exact in ritmul specificat (timp)
(1p) iesirea numaratorului se schimba in maniera necesara (valori)
rom1 (9p):
(1p) conditia de citire a memoriei este corecta
(1p) dimensiunea memoriei e corecta (numar adrese)
(1p) dimensiunea iesirii memoriei e corecta
(1p) continutul memoriei este corespunzator
(1p) intrarile sunt declarate ca intrari
(1p) iesirile sunt declarate ca iesiri
(3p) memoria e implementata corect si complet
dec1 (3p):
(1p) conditia de decodare este corecta
(2p) decodorul e implementata corect si complet
top (12 p):
(2p) memoria rom1 este instantiata corect (denumire, tip, dimensiune)
(2p) numaratorul num1 este instantiat corect (denumire, tip, dimensiune)
(2p) decodorul dec1 este instantiat corect (denumire, tip, dimensiune)
(2p) toate legaturile rom1 sunt corecte (denumire, tip, dimensiune)
(2p) toate legaturile dec1 sunt corecte (denumire, tip, dimensiune)
(2p) toate legaturile din exterior se duc spre blocurile corecte (denumire, tip, dimensiune)
design (16p):
(5p) design-ul este complet (ca numar / tip de componente) si nu are erori de sintaxa
(6p) design-ul functioneaza pe FPGA asa cum s-a cerut (intre stari trec fix. 500 milisecunde si starile se succed in ordinea ceruta)
(1p) corespondenta semnalului de ceas <> pin e corecta
(2p) corespondenta butoane <> pini e corecta
(2p) corespondenta biti de iesire <> pini e corecta
coding_style(4p)
(4p) codul este usor de citit (indentat si spatiat similar cu exercitiul din laborator5

Figure References

1. Figure 1. A digital signal (as a result of both sampling and quantization processes). Digital Integrated Circuits https://wiki.dcae.pub.ro/index.php/Introducere._Verilog_HDL
2. Figure 2. A time-sampled signal (as a result of sampling process). Digital Integrated Circuits https://wiki.dcae.pub.ro/index.php/Introducere._Verilog_HDL
3. Figure 3. A value-sampled signal (as a result of quantization process). Digital Integrated Circuits. https://wiki.dcae.pub.ro/index.php/Introducere._Verilog_HDL
4. Figure 4. Analog to digital conversion, digital processing and digital to analog conversion example. Dornelas, Helga. "Low power SAR analog-to-digital converter for internet-of-things RF receivers." (2018).
5. Figure 5. Generic FPGA Architecture Overview. https://www.eetimes.com/all-about-fpgas/
6. Figure 6. Xilinx CLB. Blue blocks are multiplexers, violet blocks are FFs and dark-green blocks are LUTs (look-up tables) https://www.eetimes.com/all-about-fpgas/
7. Figure 7. FPGA development flow. https://www.xilinx.com/applications/isolation-design-flow.html
8. Figure 8. The Nexys 4 DDR FPGA board, https://digilent.com/reference/_media/reference/programmable-logic/nexys-4-ddr/nexys4ddr_rm.pdf
9. Figure 9. Nexys 4 DDR board features, https://digilent.com/reference/_media/reference/programmable-logic/nexys-4-ddr/nexys4ddr_rm.pdf
10. Figure 10. GPIO devices on the Nexys4 DDR FPGA board. https://digilent.com/reference/_media/reference/programmable-logic/nexys-4-ddr/nexys4ddr_rm.pdf
11. Figure 11. NOT gate ("inverter") made of one pMOS (top) and one nMOS (bottom) transistor. Why do CMOS NOT gate designs differ from BJT NOT gate designs? https://electronics.stackexchange.com/questions/570389/why-do-cmos-not-gate-designs-differ-from-bjt-not-gate-designs
12. Figure 12. ANSI / IEC [5] (right) and MIL-STD-806B [6] (left) symbols foremost common 7/16 dual-input logic gates (elementary), with their names. Logic Gates. https://learnabout-electronics.org/Digital/dig21.php
13. Figure 13. The truth tables for the most commonly used logic gates. Nucleic Acid Computing and its Potential to Transform Silicon0Based Technology. https://www.researchgate.net/publication/291418819_Nucleic_Acid_Computing_and_its_Potential_to_Transform_Silicon-Based_Technology
14. Figure 14. Representing a g(n) function which asymptotically bound f(n) function. Big-O notation. https://xlinux.nist.gov/dads/HTML/bigOnotation.html

15. Figure 15. The O-notation complexity increases with the number of elements processed. O(1) and O(logn) are usually excellent complexities, O(n) is fair, and O(n*logn) is usually considered almost decent in algorithms and circuits. Big-O Algorithm Complexity Cheat Sheet (Know Thy Complexities!) @ericdrowell. https://www.bigocheatsheet.com/
16. Figure 17. Verilog syntax cheat sheet (1/2) accessed online on 12.10.2023 https://marceluda.github.io/rp_dummy/EEOF2018/Verilog_Cheat_Sheet.pdf
17. Figure 18. Verilog syntax cheat sheet (2/2) accessed online on 12.10.2023 https://marceluda.github.io/rp_dummy/EEOF2018/Verilog_Cheat_Sheet.pdf
18. Figure 19. VHDL cheat sheet (1/2) accessed online on 08.10.2023: https://vhdlweb.com/static/vhdl_cheatsheet.pdf, and www.ece.tufts.edu/es/4
19. Figure 20. VHDL cheat sheet (2/2) accessed online on 08.10.2023: https://vhdlweb.com/static/vhdl_cheatsheet.pdf, and www.ece.tufts.edu/es/4
20. Figure 21. 2-input AND gate
21. Figure 22. Verilog code (dataflow) for a 2-input AND gate
22. Figure 23. Verilog code (dataflow) for a 2-input AND gate
23. Figure 24. 4-input AND gate from 2-input AND gates (dataflow)
24. Figure 25. Verilog description for 4-input AND (dataflow)
25. Figure 27. 4-input AND gate from 2-input AND gates (structural)

References

1. C.Bira, “[Digital] Electronics by Example When Hardware Greets Software”, MATRIX ROM, October 2023, ISBN 978-606-25-0845-6, online available: https://www.researchgate.net/publication/374388893_Digital_Electronics_by_Example_When_Hardware_Greets_Software
2. https://www.iso.org/standard/31898.html accessed on 10.08.2023
3. https://www.jedec.org accessed on 10.08.2023
4. Loops & Complexity in DIGITAL SYSTEMS (Lecture notes on Digital Design in Ten Giga-Gate/Chip Era) by Gheorghe M. Stefan, link: http://users.dcae.pub.ro/~gstefan/2ndLevelteachingMaterials/0-BOOK.pdf accessed on 25.07.2023
5. "IEEE Standard Graphic Symbols for Logic Functions (Including and incorporating IEEE Std 91a-1991, Supplement to IEEE Standard Graphic Symbols for Logic Functions)," in *IEEE Std 91a-1991 & IEEE Std 91-1984,* vol., no., pp.1-160, 13 July 1984, doi: 10.1109/IEEESTD.1984.7896954.
6. MIL-STD-806B, https://bitsavers.org/pdf/mil-std/MIL-STD-806B_Graphical_Symbols_For_Logic_Diagrams_19620226.pdf accessed on 28.07.2023
7. Abels, Seth & Khisamutdinov, Emil. (2015). Nucleic Acid Computing and its Potential to Transform Silicon-Based Technology. DNA and RNA Nanotechnology. 2. 10.1515/rnan-2015-0003.
8. S.Winbers, J.Taylor, Verilog Cheat Sheet, https://marceluda.github.io/rp_dummy/EEOF2018/Verilog_Cheat_Sheet.pdf accessed on 08.10.2023
9. Thomas H. Cormen, Charles E. Leiserson, Ronald L. Rivest, and Clifford Stein. 2009. Introduction to Algorithms, Third Edition (3rd. ed.). The MIT Press.
10. C99, ISO/IEC 9899:1999 standard, https://www.iso.org/standard/29237.html accessed on 30.09.2023

Călin Bîră, PhD., is Associate Professor at the Politehnica University of Bucharest, where he teaches undergraduate and graduate courses related to programming, microcontrollers, digital design, signal acquisition and processing. He obtained his PhD in 2013 from the Politehnica University of Bucharest, with a thesis on programming environment for (energy-efficient embedded) accelerators, thus gradually shifting to an academic career. His work with the Faculty of Electronics, Telecommunications and Information Technology aims to bridge academia (research and teaching) with business and industry and their ways of designing research and development projects, thus addressing the gap between university and businesses. Călin Bîră's commitment to academic research and strengthening international collaboration and teamwork is made visible by multiple research grants and projects (DocInvest, SAVE, DEXTER, ATLAS) as well as by publications in the domain of electronics, programming and signal processing. Prior to his pursuing an academic career, Călin Bîră worked for 8 years as an engineer for global companies, specializing in low-level software and hardware design. His current interests include energy-efficient computation and embedded systems for research and commercial projects.