ELECTRONIC DEVICES AND CIRCUITS III

module MCM5/EV

Volume 1/2

THEORY AND EXPERIMENTS

***TEACHER / STUDENT** manual*

ElettronicaVeneta

"Final English version provided by cambridge Open Learning"

CONTENTS

SAFETY RULES

Keep this handbook at hand for any further help.

After the packaging has been removed, set all accessories in order so that they are not lost and check the equipment integrity. In particular, check that it shows no visible damage.

Before connecting the equipment to the +/- 12V power supply, be sure that the rating corresponds to the one of the power mains.

This equipment must be employed only for the use it has been conceived, i.e. as educational equipment, and must be used under the direct supervision of expert personnel.

Any other use is not proper and therefore dangerous. The manufacturer cannot be held responsible for eventual damages due to inappropriate, wrong or unreasonable use.

Lesson B20: Characteristic parameters of small signal amplifiers

OBJECTIVES

- Analysis of a common emitter circuit amplifier:
- calculation of the bias parameters (equivalent base resistance, equivalent bias voltage of the base-emitter junction, base current)
- measurement of the voltage gain
- influence of the coupling capacitance at the amplifier input, as a function of frequency
- measurement of the input and output resistances

EQUIPMENT REQUIRED

- base unit for the IPES system (power supply mod. PS1-PSU/EV, module holder structure mod. MU/EV), Individual Control Unit mod.SIS1/SIS2/SIS3 (this module can operate autonomously, faults are inserted through dip-swicthes available in in the module. When external control units are used, these four dip-swicthes will be set to OFF, that is downwards)
- experiment module mod. MCM5/ EV
- function generator
- oscilloscope
- multimeter.

B20.1 BASIC THEORY

Consider a transistor biased in its normal operating region. From the output curves, it can be seen that when the input current i_b varies, the output parameters i_c and v_{ce} vary, too.

So by applying an input signal i_b you obtain two output signals i_c and v_{ce} which will have the same shape of i_b, if the bias point is in the linear region and if i_b has limited amplitude, i.e. it is a "small signal" (fig.B20.1).

The current i_c, not only behaves like i_b, it is also much larger. The output signal of the transistor is said to be AMPLIFIED with respect to the input one.

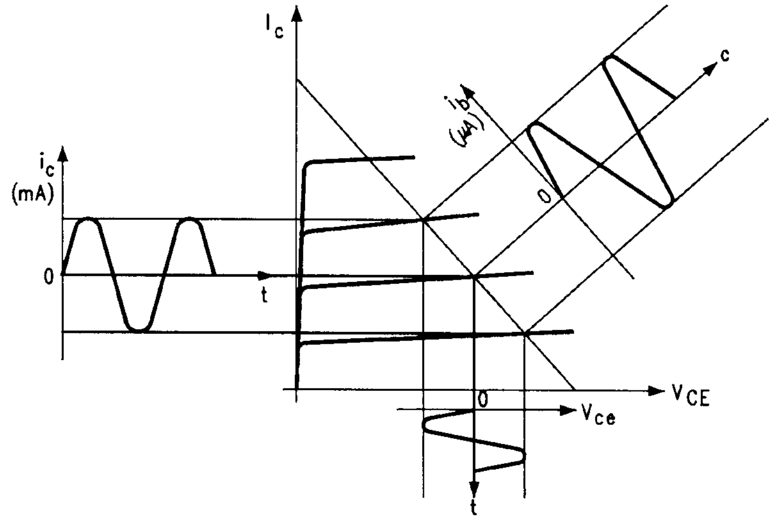


fig.B20.1

Equivalent circuit of the transistor

In the region around the operating point, the transistor parameters can be considered constant and the transistor can be represented with a linear model, called the "equivalent circuit". The model used for low frequency transistors is called the "hybrid" model, and its parameters the "h" parameters.

With this model, the transistor is represented as a four terminal system (in figure B20.2 the common emitter transistor is used as example) characterized by four electrical variables: the input voltage v_i and current i_i; the output voltage v_o and the current i_o.

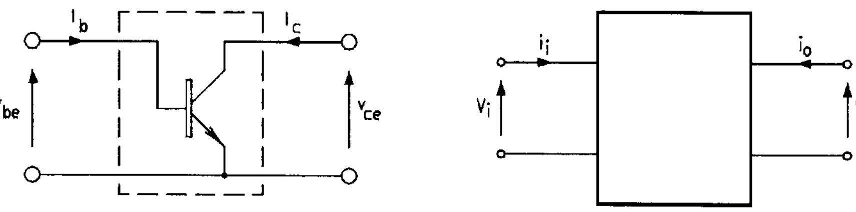


fig. B20.2

Equivalent circuit of the common emitter transistor

The h parameters used for the equivalent circuit of the common emitter transistor (figure B2 0.3) are:

h_{ie} h_{oe} h_{fe} h_{re}

where the subscripts have the following meaning: e = emitter
i = input o = output
f = forward r = reverse

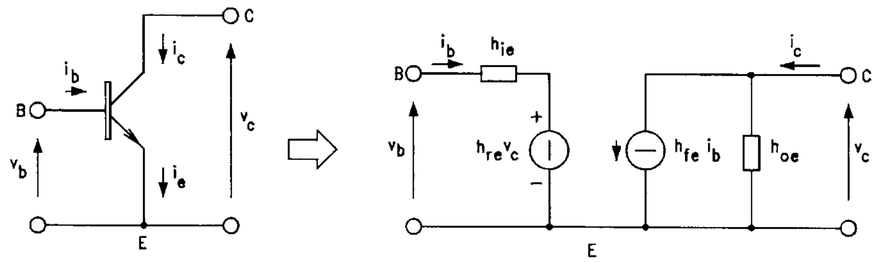


fig. B20.3

The ***h*** parameters are defined as follows:

$$h_{ie} = \frac{\Delta v_{be}}{\Delta i_b} \quad [\ v_{ce} = \text{const}\ ]$$

h_{ie} is the ratio of variations in the base-emitter voltage to the variations of the base current, with the collector-emitter voltage constant. Its dimensions are those of a resistance, expressed in Kohm and is approximately $h_{fe}.25/I_{CQ}$, with I_{CQ} in Amps (I_{CQ} is the dc bias current in the collector)

$$h_{oe} = \frac{\Delta i_c}{\Delta v_{ce}} \quad [\ i_b = \text{const}\ ]$$

this is the ratio between collector current variations and variations in the collector-emitter voltage, with a constant base current. Dimensionally it is a conductance and can be some tens of μmho.

$$h_{fe} = \frac{\Delta i_c}{\Delta i_b} \quad [\ v_{ce} = \text{const}\ ]$$

this is a current gain, and is the ratio between collector current variations and base current variations, with a constant collector-emitter voltage. It is a pure number and can vary from some tens to some hundreds. It depends on I_{CQ}

$$h_{re} = \frac{\Delta v_{be}}{\Delta v_{ce}} \quad [\ i_b = \text{const}\ ]$$

this is the ratio between the variations of the base-emitter voltage and the variation of the collector-emitter voltage, with the base current constant. It is a pure number which can vary from 10^{-3} to 10^{-4}.

Equivalent circuit of the common collector transistor

The equivalent circuit is shown in fig.B20.4. These h parametersare defined analogously to those of the common emitter, and the subscript "c" means collector. The relations between the h parameters of the common emitter and common collector are:

$h_{ic} = h_{ie} \quad h_{rc} = 1\text{-}h_{re} \quad h_{oc} = h_{oe} \quad h_{fc} = 1+h_{fe}$

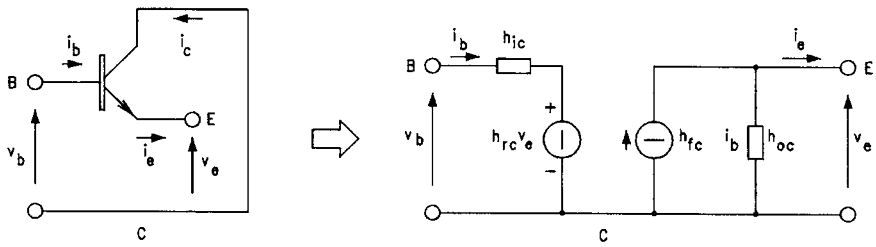


fig.B20.4

Equivalent circuit of the common base transistor

The equivalent circuit is shown in fig.B20.5. These h parameters are defined analogously to the common emitter ones, and the subscript "b" means base. The relations between the h parameters of the common emitter and common base transistors are:

$h_{ib} = h_{ie}/(1+h_{fe}) \qquad h_{rb} = h_{ie}\cdot h_{oe}/(1+h_{fe}) - h_{re}$

$h_{ob} = h_{oe}/(1+h_{fe}) \qquad h_{fb} = h_{fe}/(1+h_{fe})$

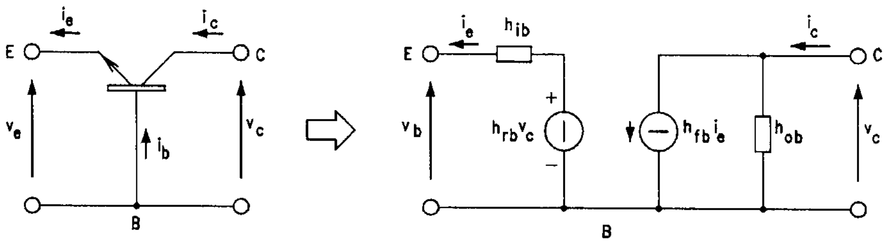


fig.B20.5

Variations in the h parameters

The h parameters depend on 3 main factors:

- transistor operating point
- temperature
- frequency.

As an example figure B20.6 shows h_{ie}, h_{fe}, h_{re}, h_{oe} as function of the bias current I_{CQ}. The parameters are normalized in respect to the values when I_{CQ} = 1 mA.

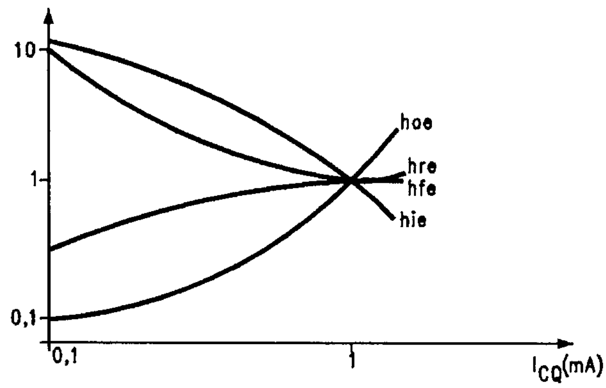


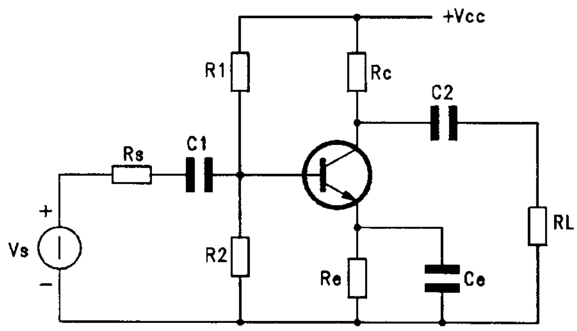
fig.B20.6

Characteristics of a common emitter amplifier as function of the h parameters

Figure B20.7 shows the normal common emitter amplifier. R1, R2 and Re constitute the bias network. v_s and Rs represent the generator and its internal resistance.

Considering the circuit only for small signal variations (ac), the capacitors are practically a short-circuit. From the original circuit, you can obtain the so called DYNAMIC CIRCUIT, which represents the amplifier only for the ac or signal components. Notice that Vcc, which doesn't present any variation, can be considered as connected to ground, thus obtaining (in the dynamic circuit) R1 in parallel with R2 and Rc in parallel with R_L. In the diagram we set R_B = R1//R2 and Rp = Rc//R_L (total load).

A)



B)

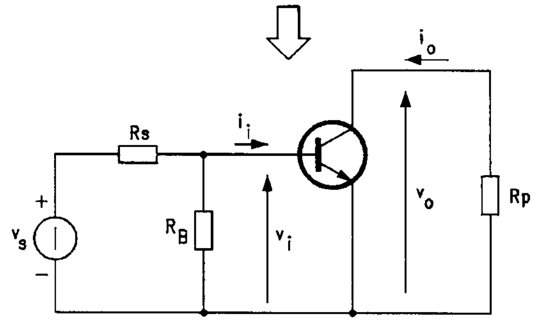


fig.B20.7

Replacing the transistor with its equivalent circuit, the amplifier can be represented by figure B20.8.

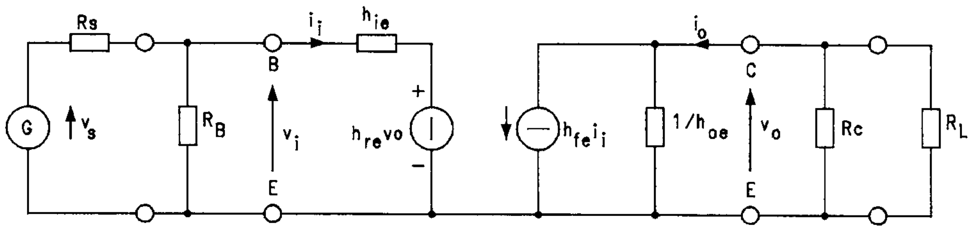


fig. B20.8

An analysis of this equivalent circuit enables the different dynamic variables of the amplifier to be calculated.

1. *Current gain A_i:*

$$A_i = \frac{i_o}{i_i} = \frac{h_{fe}}{1 + h_{oe} \cdot R_p}$$

where $Rp = Rc//R_L$

As the product ($h_{oe} \cdot R_p$) is negligible in comparison to 1, the current gain is approximately equal to h_{fe}:

$A_i \approx h_{fe}$

2. *Input resistance R_i:*

$R_i = v_i/i_i = h_{ie} + h_{re} \cdot R_p \cdot A_i$
As h_{re} is very small, if $(h_{re} \cdot R_p \cdot A_i)$ is negligible in respect to h_{ie} you obtain:

$R_i = h_{ie}$

3. *Voltage gain A_V:*

$$A_v = \frac{v_o}{v_i} = \frac{R_p}{R_i} \cdot A_i$$

Using the simplified relations for A_i and R_i, you obtain:

$A_V = -R_p \cdot h_{fe}/h_{ie}$

4. *Total gain A_{vt}:*

The generator connected to the input of the amplifier, has an internal resistance Rs which causes a voltage drop across it when supplying current to the circuit (figure B20.9). The attenuation ratio due to Rs, is:

$$\alpha = \frac{v_i}{v_s} = \frac{R_{it}}{Rs + R_{it}}$$

where $R_{it} = R_B \,//\, R_i$ is the total input resistance of the amplifier.
The total voltage gain is then equal to:

$A_{vt} = v_o/v_s = \alpha \cdot A_V$

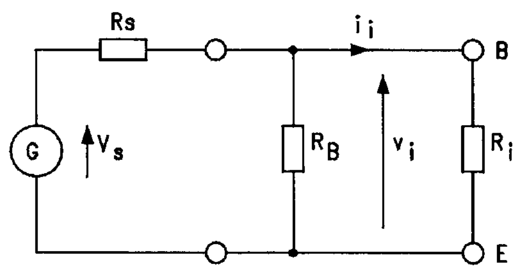


fig.B20.9

5. *Output resistance R_O*:

$$R_o = \frac{v_o}{i_o} = \frac{1}{h_{oe} - \dfrac{h_{fe} \cdot h_{re}}{h_{ie} + R_s'}}$$

where Rs' = R_B // Rs with Rs as the internal resistance of the input signal generator. The total output resistance of the amplifier is $R_{ot} = R_O$ // Rc.

6. *Power gain A_P*:

$A_P = A_i \cdot A_V$

Using the simplified relations gives:

$A_P = R_P \cdot h_{fe}^2 / h_{ie}$

7. *Behaviour of A_i, A_V, A_P as function of the load.*

For the following typical values of hybrid parameters:

$h_{ie} = 1000\ \Omega$, $h_{re} = 0.0001$, $h_{fe} = 100$, $1/h_{oe} = 10000\ \Omega$

the behaviours of the amplifier gains are shown in figure B20.10.

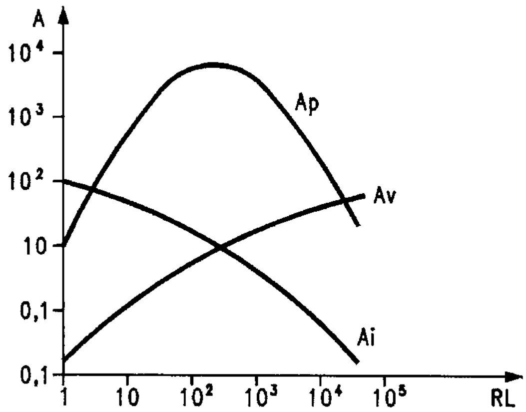


fig.B20.10

The graphs show that the current gain drops as the load resistance R_L increases. However Av increases, and so the power amplification increases to reach a maximum and then it rapidly drops. The max. power value is obtained with R_L = Ro.

NOTE 1: For the analytic study of the dynamic circuit, in common collector or common base amplifiers, proceed as in the last example, using the h parameters corresponding to the configuration under test.

NOTE 2: The manufacturers usually supply the following h parameters: h_{fe}, h_{ib}, h_{rb} and h_{ob}. The common emitter parameters are then found from the following:

$h_{ie} = h_{ib} \cdot (h_{fe} + 1)$

$h_{oe} = h_{ob} \cdot (h_{fe} + 1)$

$h_{re} = -h_{rb} + (h_{ib} \cdot h_{ob}) \cdot (h_{fe} + 1)$

8. *Cut-off frequency due to the coupling capacitors.*

The capacitors in the circuit determine the lower limit of the last formula. Considering that the capacitances C1, C2 and Ce, the equivalent circuit of the figure B20.8, neglecting h_{oe} and h_{re}, becomes as shown in fig.B20.11.

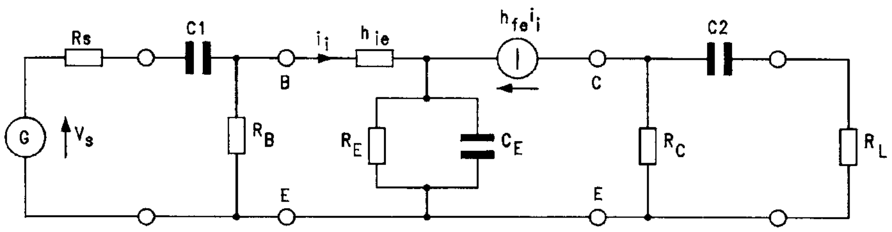


fig. B20.11

You can detect the lower cut-off angular frequency w_L, approximately, from the following relations which are true only if $C_E \cdot R_E >> t1$ (normal operating region):

$\tau 1 = C1 \cdot R_{eq1}$ with $R_{eq1} = Rs + (R_B // h_{ie})$

$\tau 2 = C_E \cdot R_{eqe}$ with $R_{eqe} = R_E // R_{ue}$

$R_{ue} = (Rs' + h_{ie}) / (1 + h_{fe})$

$Rs' = //Rs$

$1/t1 = (1/\tau 1) + (1/\tau 2)$

$t2 = C2 \cdot (Rc + R_L)$

A. if $t1 \neq t2$, $w_L = \sqrt{[(1/t1)^2)+(1/t2)^2]}$

B. if $t1 = t2$, $w_L = 1.55/t1$

At high frequencies, the different capacitances inside the transistor are no longer negligible, and the equivalent low frequency circuit used here is not applicable.

The equivalent circuit at high frequencies of the common emitter, is called the Giacoletto or "π"circuit.

B20.2 EXERCISES

➲ *MCM5*	**Disconnect all jumpers** **Set in OFF all S switches**
➲ *SIS1*	**Turn all switches *OFF***
➲ *SIS2*	**Insert lesson code: B20**

Calculation of the bias parameters

- Insert jumpers J3, J5, J6, J17, J11, J13, J26, connect the multimeter (function IDC) between terminals 4 and 5, adjust RV1 completely C.W. (zero Ω) to produce the circuit of figure B20.12

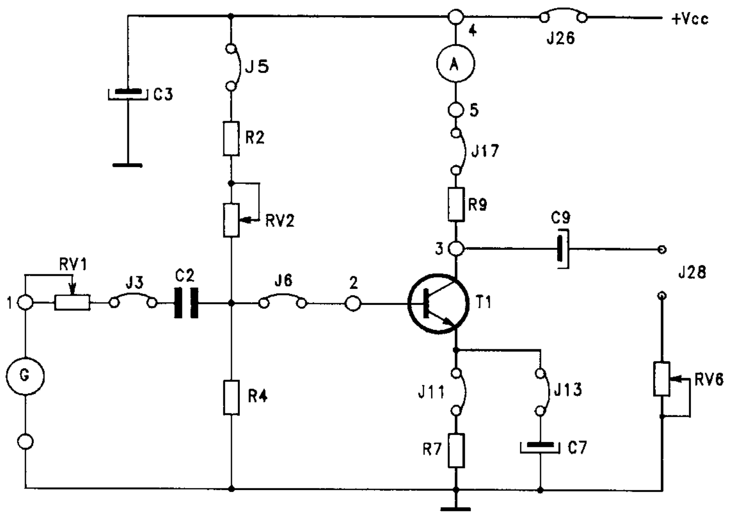


fig. B20.12

- Set Vcc adjustable power supply to 20V.
- Adjust the trimmer RV2 to obtain I_{CQ} = 10 mA
- turn off the power supplies and remove jumper J5
- now measure the resistance of the trimmer RV2
- once RV2, R2 and R4 are known, calculate the equivalent resistance R_B of the base bias (refer to Fig B20.7)

Q1 *What is approximately?*

SET

A	*B*	
1	5	33 KΩ
2	4	10 KΩ
3	1	some tens of ohms
4	3	some KΩ
5	2	it lies between 100 KΩ and 500 KΩ

- Calculate the equivalent dc voltage of the base-emitter circuit V_{BB} = $(R4 \cdot Vcc) / (RV2 + R2 + R4)$
- the base current is $I_{BQ} = (V_{BB} - V_{BEQ} - R7 \cdot I_{EQ})/RB$ where $V_{BE} = 0.6$ V and $I_{EQ} = I_{CQ}$. Calculate the base bias current I_{BQ}
- calculate the static (d.c.) current gain , (I_{CQ} / I_{BQ})

Measurement of the amplification and effect of the input capacitance

- Insert jumper J5
- Vary RV6 load completely C.W. (max. resistance value) and connect it to the amplifier by inserting J28.
- Connect the oscilloscope channel 1 at terminal 2 (T1 base transistor) and the channel 2 across the RV6 load.
- Connect at terminals 1 and ground the the function generator with a sine signal, 1 KHz, vary the amplitude to check 20 mVpp at terminal 2.
- Using the values of the voltages measured with the oscilloscope, calculate the voltage amplification $Av = v_{out}/v_{in}$
- Check the phase shift between input and output signals.
- Move the channel 1 of the oscilloscope between RV1 and C2 to display the signal before the capacitor.
- Evaluate the voltage amplification under these conditions.

The amplification obtained is lower, due to the attenuation of the input signal caused by capacitor C2. At a frequency of 1 KHz in fact C2 has a reactance of about 1.5 KΩ, and this value is similar to the input resistance R_{it} of the amplifier.

- Replace C2 with C1, removing J3 and inserting J2
- Observe that the attenuation introduced is now smaller.

X_{C1} is about 16 Ω, which is much smaller than R_{it} of the amplifier

- Gradually increase the frequency of the input signal and check if the circuit amplification remains constant.

Measurement of the input and output resistances

- Set the input signal with sine wave and 1KHz, vary the amplitude to check 20 mVpp at terminal 2. Display the signal across the load RV6 on the oscilloscope.
- Gradually increase the resistance of RV1 so that the voltage across the RV6 load is reduced to half its initial value.
- Disconnect the function generator and remove the jumper J2. With an ohmmeter, measure the inserted resistance of RV1, which in these conditions is equal to the total input resistance of the amplifier $R_{it} = R_B // Ri$

Q2 *What is R_{it} ?*

SET

A	*B*	
1	4	equal to R_i
2	3	infinite
3	2	a few Kohm
4	5	a few ohms
5	1	a few Mohm

- Vary RV1 completely C.W. (minimum resistance), insert jumper J2 and remove J28.
- Connect again the function generator with a sine wave, 1 KHz, vary the amplitude to check 20 mVpp at terminal 2.
- Measure the amplitude of the signal after the capacitor C9.
- Insert J28 and progressively lower RV6, to reduce the output voltage by half.
- Remove jumper J28 and, with an ohmmeter, measure the resistance of the load RV6; which in this condition is equal to the total output resistance R_{ot} of the amplifier ($R_{ot}= R_o // Rc$)

Q3 *What is R_{ot} ?*

SET

A	*B*	
1	2	about 1 Kohm
2	5	many Kohm
3	1	a few ohm
4	3	infinite
5	4	many Mohm

B20.3 SUMMARY QUESTIONS

Q4 *The h parameters are used to describe the operation of an amplifier:*

SET

A	*B*	
1	2	using small signals
2	4	at high frequencies
3	5	at low frequencies
4	1	with small signals and at low frequencies
5	3	with d.c. current

Q5 *In an amplifier equivalent circuit:*

SET

A	*B*	
1	3	the d.c. components are not included
2	4	the a.c. components are not included
3	1	the d.c. as well as the a.c. current flows
4	5	the load is disconnected
5	2	the biasing network is not included

Q6 *Find the current gain* A_i *of a common emitter transistor amplifier, with:* $h_{fe} = 100$; $h_{ie} = 1\ K\Omega$; $1/h_{oe} = 40\ K\Omega$; $R_L = 45\ K\Omega$; $Rc = 500\ \Omega$

SET

A	*B*	
1	6	500
2	1	40 KΩ
3	4	98
4	5	50
5	2	20
6	3	200 μF

Q7 *Find the voltage gain* A_v *of the amplifier in Q6:*

SET

A	*B*	
1	4	48
2	3	-100
3	6	-48
4	4	100
5	1	75
6	2	-75

Lesson B21: The EMITTER FOLLOWER

OBJECTIVES

- Analytic study of an emitter follower circuit as function of its ***h*** parameters:
  - calculation of the current gain Ai
  - calculation of the input resistance Ri
  - calculation of the voltage gain Av
  - calculation of the output resistance Ro
- Experimental study of the circuit:
  - measurement of the voltage gain
  - measurement of the phase difference between input and output signal
  - measurement of the input resistance Rit of the amplifier

EQUIPMENT REQUIRED

- base unit for the IPES system (power supply mod. PS1-PSU/EV, module holder structure mod. MU/EV), Individual Control Unit mod.SIS1/SIS2/SIS3 (this module can operate autonomously, faults are inserted through dip-swicthes available in in the module. When external control units are used, these four dip-swicthes will be set to OFF, that is downwards)
- experiment module mod. MCM5/ EV
- function generator
- oscilloscope
- multimeter.

B21.1 BASIC THEORY

An emitter follower amplifier is a circuit in which the common terminal across the input and output is the collector. (This circuit is also called common collector amplifier). Figure B21.1 shows a typical emitter follower. Note that the load is connected to the emitter.

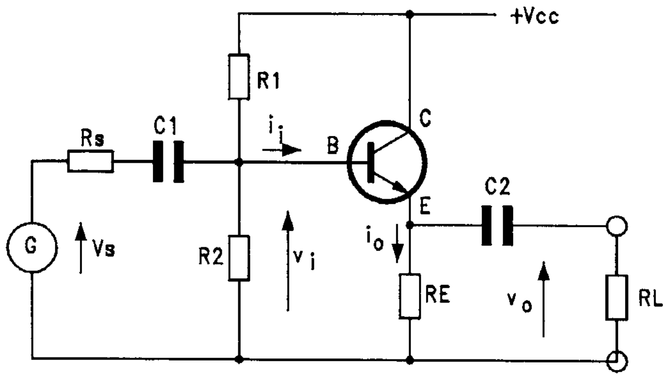


fig.B21.1

The characteristics of this kind of amplifier are as follows:
1. voltage gain is slightly less than 1
2. small output resistance
3. high input resistance
4. output signal is in phase with the input signal.

The fact that this circuit has a high input resistance and a low output resistance makes it useful as a buffer stage between a high resistance source and a low resistance load.

The name of the follower comes from the fact that the voltage gain is positive and slightly lower than unity. A rise, for example, of the input signal becomes an equal rise in the output signal. The output "follows" the input.

Biasing

The load line is determined by the following equation:

$$Vcc = V_{CE} + R_E \cdot I_C$$

The bias resistors are R1, R2 and R_E.

Characteristics as function of the h parameters

The analytic study of the amplification requires the use of the transistor equivalent circuit. The emitter follower of the figure B21.1 is shown, for small signal applications, in the diagram of figure B21.2.

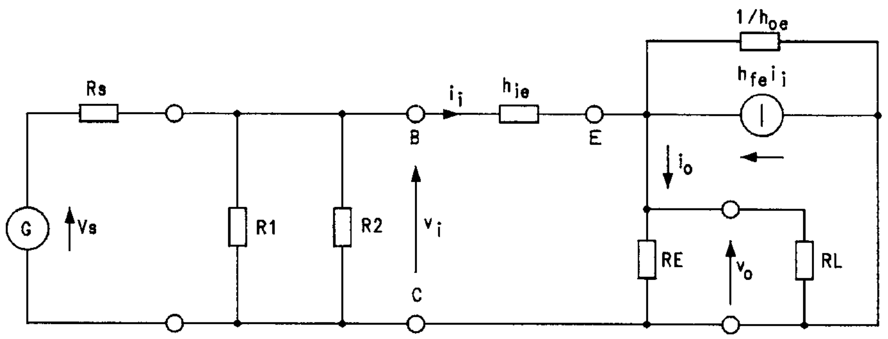


fig. B21.2

The bias resistances R1 and R2 can be substituted by a base equivalent resistance: $R_B = R1//R2$.

An analysis of the equivalent circuit gives the following parameters:

1. *Current gain A_i*

$$A_i = \frac{i_o}{i_i} = \frac{1 + h_{fe}}{1 + h_{oe} \cdot R_p}$$

where $R_p = R_E // R_L$

When the product $(h_{oe} \cdot R_p)$ is much less than 1, the current gain is almost equal to h_{fe}:

$A_i \approx h_{fe}$

2. *Input resistance R_i*

$R_i = v_i/i_i = h_{ie} + R_p \cdot A_i$

As $R_p \cdot A_i$ is usually much greater than h_{ie}, the last equation becomes:

$R_i \approx R_p \cdot A_i$

3. *Voltage gain A_V*

$A_V = v_o/v_i = 1 - h_{ie}/R_i$

As you can note, the gain is always less than unity and has a positive sign. With the same Rp, if the collector current increases the gain becomes closer to 1.0. In fact h_{ie} drops, while h_{fe} and Ai are practically unaffected by the variation of I_C over a wide range.

4. *Total voltage gain A_{vt}*

The generator connected to the input of the amplifier has an internal resistance, causing an internal voltage drop when it supplies current to the circuit (figure B21.3). The attenuation of the signal given by :

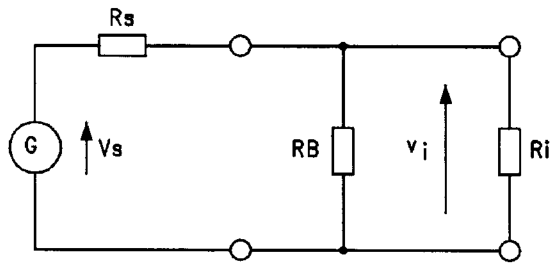


fig.B21.3

$\alpha = v_i/v_s = R_{it}/(R_s + R_{it})$

where $R_{it} = R_B // R_i$ is the total input resistance of the amplifier. Unlike the common emitter amplifier, R_i is generally much greater than R_B and Rs. So α is almost 1.0. The total gain is:

$A_{vt} = v_o / v_s = \alpha \cdot Av$

with $A_{vt} < Av < 1$

5. *Output resistance R_{ot} seen from the load R_L*

$$R_{ot} = \frac{v_L}{i_L} = \frac{1}{\dfrac{1}{R_e} + h_{oe} + \dfrac{1+h_{fe}}{h_{ie} + R_{st}}}$$

where $R_{st} = R_B$ // Rs, with Rs internal resistance of the input signal generator.

Usually h_{fe} is very big and h_{oe} is very small. The last formula then becomes:

$R_{ot} = R_E$ // [($h_{ie} + R_{st}$) / h_{fe}]

From this we find that the minimum output resistance is obtained with Rst = 0. In this case, since h_{ie} is in the order of KΩ and h_{fe} is typically 100, the output resistance is less than 10 Ohms:

$R_{ot} = R_E$ // 10 Ω

The following table shows the main differences between the emitter follower and the common emitter connection:

	Common emitter	Emitter Follower
Ri	small	high
Av	>> 1	unity
Ro	big	very small

B21.2 EXERCISES

➲ *MCM5*	**Disconnect all jumpers** **Set in OFF all S switches**
➲ *SIS1*	**Turn all switches *OFF***
➲ *SIS2*	**Insert lesson code: B21**

Voltage gain

- Insert jumpers J1, J2, J6, J5, J12, J19, J26, the multimeter (function IDC) between terminals 4 and 5 to produce the circuit of figure B21.4

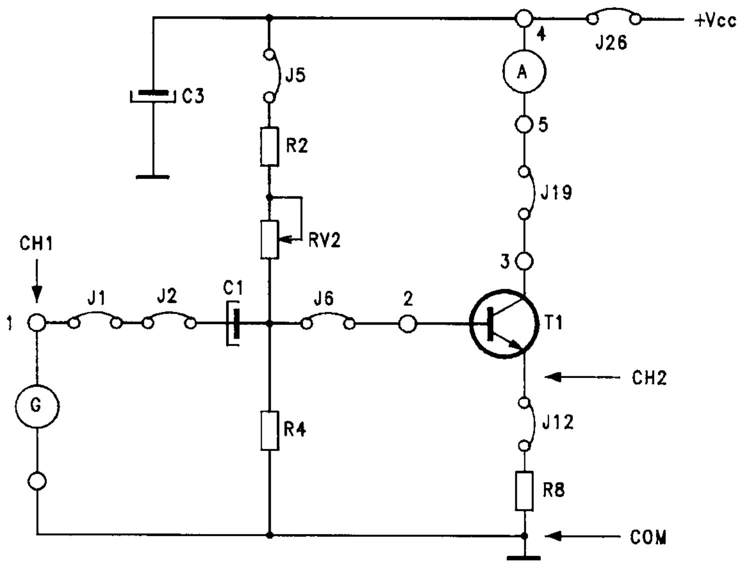


fig.B21.4

- Set Vcc adjustable power supply to 20V.
- Adjust trimmer RV2 to bias the transistor with $I_{CQ} \approx 5$ mA
- Connect the function generator at terminals 1 and ground with sine wave signal, 1 KHz and 4 V peak-to-peak.
- Connect the oscilloscope channel 1 at terminal 1 to display the input signal and the channel 2 at terminal 6 to display the output signal across R8.
- Determine the voltage gain, and the phase between the two displayed signals.

Q1 *What is the voltage gain Av ?*

SET

A	*B*	
1	6	it takes values ranging between 1 and 1.5
2	3	some tens of millivolt
3	5	some handred of millivolt
4	1	it takes values between 0.9 and 1
5	2	more than 10
6	4	none of the above

Q2 *What is the phase difference between the output and input signal?*

SET

A	*B*	
1	4	it takes values between 150 and 220 degrees
2	5	a few degrees
3	2	almost zero
4	3	180 degrees
5	1	none of the above

Input resistance measurement

- Remove jumper J1 so to add the trimmer RV1 in series with the circuit. Vary RV1 completely C.W. (minimum resistance).
- Connect the oscilloscope channel 1 between RV1 and C1 and channel 2 at terminal 6.
- Increase the RV1 value so that the signal on channel 1 is halved.
- Turn off the generator, remove jumpers J2.
- Measure the resistance of the trimmer, which now corresponds to the input resistance R_{it} of this circuit. Note that R_{it} is influenced by the base bias network. Higher values of R4-R2 will produce higher R_{it}

- Turn on the function generator and insert again jumpers J1, J2.

➲ *SIS1*	**Turn switch SW3 *ON***
➲ *SIS2*	**Press *INS***

Q3 *What effect do you see on the output signal?*

SET		
A	*B*	
1	3	the amplitude increases
2	5	the amplitude decreases
3	4	the frequency varies
4	2	it is distorted on the positive half-waves
5	1	it is distorted on the negative half-waves

Q4 *What is the reason for this effect?*

SET		
A	*B*	
1	5	a variation of h_{fe} of the transistor
2	2	a variation of the amplifier gain
3	4	a variation of the operating point due to the reduction of RV2
4	3	a variation of the operating point due to the reduction of R4
5	1	a variation of the resistance connected to the emitter

➲ *SIS1*	**Turn switch SW3 *OFF***

B21.3 SUMMARY QUESTIONS

Q5 *What is the other name of an emitter follower amplifier?*

SET

A	*B*	
1	3	common base circuit
2	4	common collector circuit
3	1	common emitter circuit
4	5	dual-load circuit
5	2	resonant load amplifier

Q6 *In the emitter follower, the voltage gain and output signal phase shift are:*

SET

A	*B*	
1	4	voltage gain slightly lower than 1 and 180° shift
2	5	voltage gain slightly lower than 1 and 0° shift
3	1	voltage gain higher than 1 and 180° shift
4	3	voltage gain higher than 1 and 0° shift
5	6	voltage gain equal to 1 and 0° shift
6	2	none of the above

Q7 *Input resistance Ri and output resistance Ro are:*

SET

A	*B*	
1	6	Ri high and Ro very low
2	3	Ro equal to Ri
3	1	Ri low and Ro high
4	2	Ri and Ro both high
5	4	Ri and Ro both low
6	3	Ri practically null, Ro practically infinite

Q8 *The emitter follower is used as:*

SET

A	*B*	
1	4	voltage amplifier
2	1	phase inverter
3	2	impedance matcher
4	5	frequency multiplier
5	3	triangular wave generator

Lesson B22: The DUAL-LOAD AMPLIFIER

OBJECTIVES

- Analytic study of a circuit amplifier with dual-load as function of the h parameters:
  - calculation of the current gain Ai
  - calculation of the input resistance Ri
  - calculation of the voltage gain Av
  - calculation of the output resistances Ro
- Experimental study of the circuit:
  - measurement of the voltage gain
  - measurement of the phase difference between input and output signals
  - measurement of the phase shift between the collector signal and the emitter signal

EQUIPMENT REQUIRED

- base unit for the IPES system (power supply mod. PS1-PSU/EV, module holder structure for modules mod. MU/EV), individual control unit mod. SIS1/SIS2/SIS3
- experiment module mod. MCM5/ EV
- function generator
- oscilloscope
- multimeter.

B22.1 BASIC THEORY

A dual-load amplifier is a circuit in which the load is divided into two parts, respectively connected to the collector and emitter (figure B22.1).

The output at the collector is characterized by:
- the voltage gain can be much higher than 1
- the signal is in phase opposition to the input signal
- the output resistance is high.

The emitter output is characterized by:
- the voltage gain is slightly less than 1
- the output resistance is small
- the output signal is in phase with the input.

Setting $R_C = R_E$ the a.c. components at R_C and R_E are the same: the two output signals are in phase opposition but of equal amplitude. The two outputs are balanced, and this circuit is called a "phase inverter".

The biasing load line is given by the following equation:

$$Vcc = V_{CEQ} + (Rc + R_E) \cdot I_{CQ}$$

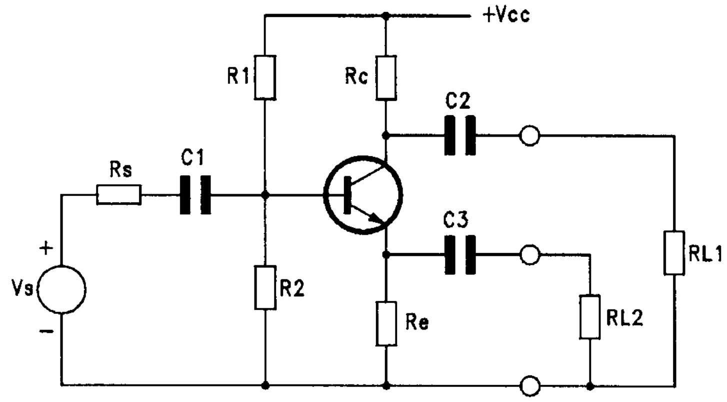


fig.B22.1

Characteristics as function of the h parameters

To analyze the amplifier, the equivalent circuit of the transistor is needed. The dual load amplifier of figure B22.1 becomes, for small signals and low frequency, equivalent to the one shown in figure B22.2.

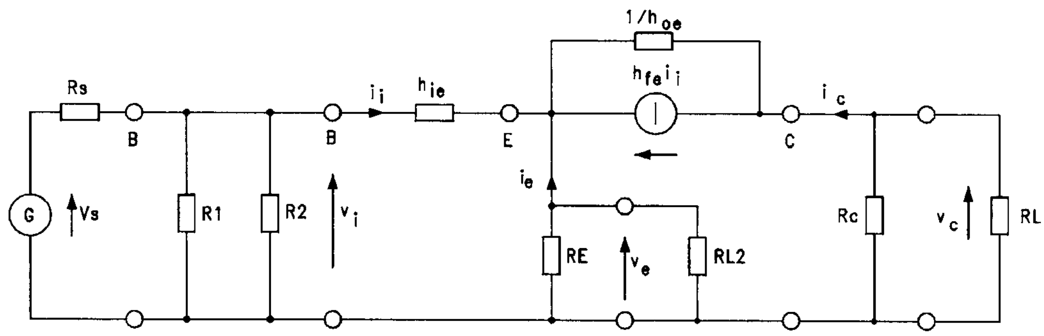


fig. B22.2

The biasing resistances R1 and R2 can be grouped together as an equivalent base resistance: R_B = R1//R2. The analytic study of the equivalent circuit allows the calculation of the dynamic characteristics:

1. *Current gains A_{ic} and A_{ie}*

   $A_{ic} = i_c / i_i = h_{fe} / [1 + h_{oe} \cdot (R_{pc} + R_{pe})]$

   where $R_{pc} = Rc \,//\, R_{L1}$, $R_{pe} = R_E \,//\, R_{L2}$

   $A_{ie} = i_e / i_i = 1 + A_{ic}$

   As A_{ic} is generally much greater than 1, then:

   $A_{ie} \approx A_{ic}$

2. *input resistance Ri*

   $Ri = v_i / i_i = h_{ie} + R_{pe} \cdot A_{ie}$

   As $R_{pe} \cdot A_{ie}$ is usually much greater than h_{ie}, this becomes:

   $Ri = R_{pe} \cdot A_{ie}$

3. *Voltage gains A_{vc} and A_{ve}*

   $A_{vc} = v_c / v_i = -R_{pc} \cdot A_{ic} / Ri$

   $A_{ve} = v_e / v_i = R_{pe} \cdot A_{ie} / Ri = 1 - h_{ie} / Ri$

   If $h_{ie} << R_{pe} \cdot A_{ie}$ then:

   $A_{vc} = -R_{pc} / R_{pe}$

   $A_{ve} = 1$

4. *Output resistances R_{oc} and R_{oe}*

   $R_{oc} \approx Rc$

   If $R_{pc} << 1/h_{oe}$, then:

   $R_{oe} \approx (h_{ie} + R_{st}) / h_{fe}$

The following table shows the main differences between the amplifiers in common emitter, emitter follower, dual-load configurations.

	Common emitter	Common collector	Dual-load
R_i	low	high	high
A_{vc}	>>1	-------	$-R_{pc} / R_{pe}$
A_{ve}	-------	unity	unity
R_{oc}	high	-------	Rc
R_{oe}	-------	low	low

As you can note, in the dual-load amplifier the voltage gain is independent on the ***h*** parameters (which may vary even for transistors of the same type), and is determined only by the external resistors.

B22.2 EXERCISES

➲ *MCM5*	**Disconnect all jumpers** **Set in OFF all S switches**
➲ *SIS1*	**Turn all switches *OFF***
➲ *SIS2*	**Insert lesson code: B22**

Voltage gains and phase shifts

- Insert jumpers J1, J2, J5, J6, J12, J17, J26, the multimeter (function IDC) between terminals 4 and 5 to produce the circuit of fig.B22.3.

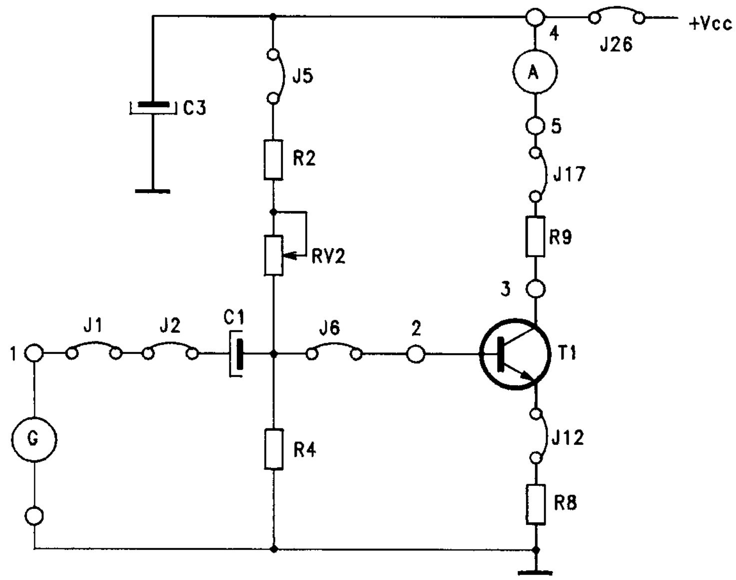


fig. B22.3

- Set Vcc adjustable power supply to 20V.
- Set Vcc=20V. Adjust trimmer RV2 to bias the transistor for $I_{CQ} \approx 5$ mA
- Connect the function generator at terminals 1 and ground with a sine wave, 1 KHz and 2 V peak-to-peak.
- Connect the oscilloscope to display the input signal and the output signals on T1 collector and emitter.
- determine the voltage gains A_{vc} and A_{ve}

Q1 *What are the two voltage gains?*

SET

A	*B*	
1	2	the 2 gains are equal
2	4	A_{vc} is double A_{ve}
3	1	$A_{vc} = 0$ and $A_{ve} = 40$
4	5	A_{vc} is half A_{ve}
5	3	$A_{vc} = 40$ and $A_{ve} = 0$

- Evaluate the phase shift between the input signal and the output Signal

Q2 *What is the phase shift between the two output signals?*

SET

A	*B*	
1	3	almost zero
2	1	slightly more than 90°
3	5	approximately 180°
4	2	approximately 120°
5	4	approximately 30°

➲ *SIS1*	**Turn switch SW12 *ON***
➲ *SIS2*	**Press *INS***

Q3 *What change has occurred?*

SET

A	*B*	
1	6	the collector resistance R9 has been increased
2	1	the emitter resistance R8 has been increased
3	2	the emitter resistance R8 has been decreased
4	5	the power supply voltage has been changed
5	3	the voltage of the signal generator has been decreased
6	4	the frequency of the output signals has been changed

➲ *SIS1*	**Turn switch SW12 *OFF***

Measurement of the input resistance Rit

- With reference to the last circuit, set the function generator with sine wave, 1 KHz and 2 V peak-to-peak.
- display on the oscilloscope the generator voltage and the voltage on the base of T1
- remove jumper J1 to insert the trimmer RV1 between the generator and C1
- increase the value of RV1 until the input signal on the base of T1, reduces to half
- turn off the function generator and remove jumper J2; measure the resistance inserted by the trimmer RV1

This value corresponds to the total input resistance R_{it} of the amplifier. R_{it} is much less than R_i, due to the bias resistors R1-R2 which are in parallel to R_i.

B22.3 SUMMARY QUESTIONS

Q4 *In a dual-load amplifier, the loads are connected to:*

SET

A	*B*	
1	5	the base and the collector
2	1	the collector and the emitter
3	2	the emitter and the base
4	3	they are in parallel and conneceted to the collector
5	4	they are in series and connected between base and emitter

Q5 *What is the input resistance of a dual-load amplifier?*

SET

A	*B*	
1	3	very low
2	5	very high
3	2	equal to the output resistance of the emitter
4	1	in the order of some tens of ohm
5	4	in the order of Mohm

Q6 *What are the output resistances, on the collector and the emitter, for a dual-load amplifier?*

SET

A	*B*	
1	5	they are exactly equal and very low
2	3	collector output resistance is equal to Rc, and the emitter resistance is low
3	6	they are exactly equal and very high
4	1	the collector output resistance is very low and the emitter istance very high
5	2	the collector output resistance is high and the emitter ance is zero
6	4	each resistance is equal to the input resistance

Q7 *Determine the gains of the dual-load amplifier, for which :*

$h_{fe} = 50$ $h_{ie} = 1.1K\Omega$ $h_{re} = 0.00025$ $1/h_{oe} = 40K\Omega$

$Rs = 0\Omega$ $Rc = 10K\Omega$ $R_E = 1K\Omega$

$R1 = 30K\Omega$ $R2 = 1.8K\Omega$

SET

A	*B*		
1	4	$A_{ie} = -20$	$A_{vc} = -9$
2	3	$A_{ic} = 40$	$A_{vc} = 9$
3	1	$A_{vc} = -9$	$A_{ve} = 0.97$
4	5	$A_{vc} = 1$	$A_{ve} = 1$
5	2	$A_{vc} = 20$	$A_{ve} = -103$

Lesson B23: RC COUPLING

OBJECTIVES

- Study of a two-stage amplifier circuit with RC coupling:
- measurement of the voltage gains
- determination of the phase difference between input and output signals

EQUIPMENT REQUIRED

- base unit for the IPES system (power supply mod. PS1-PSU/EV, module holder structure for modules mod. MU/EV), individual control unit mod. SIS1/SIS2/SIS3
- experiment module mod. MCM5/ EV
- function generator
- oscilloscope
- multimeter.

B23.1 BASIC THEORY

The purpose of an amplifier is to allow the max. possible amplification without distortion. If a single stage cannot provide sufficient amplification, it is possible to connect in cascade extra amplification stages possibly of a different kind.

For example, when a high gain and high input impedance amplifier is required, a common collector BJT can be used as first stage (high input resistance), and a common emitter BJT as second stage (high amplification).

The overall characteristics of circuits with several stages are found from the characteristics of each stage. The following table sums up typical data for the three main types of amplifier.

	Common base	Common collector	Common emitter
Input Impedance	very low	very high	low
Output impedance	high	very low	high
Current gain	unity	high	high
Voltage gain	can be very high (positive)	unity (positive)	can be high (negative)
Power gain	high	high	very high

Choice of the number, and type of stages

The choice of the number of stages, their kind, and their order, is mainly determined by the generator resistance, the load resistance, and the gain required. Most amplifiers to be obtained require:

- a high input resistance, compared to the generator resistance
- a small output resistance, compared to the load resistance

Types of couplings, or interconnection between stages

There are three types of coupling possible between stages: direct coupling, RC coupling, and transformer coupling.

RC coupling

In a multi-stage amplifier, an RC coupling is when the connection between one stage and the next is achieved with a capacitor. C2 in figure B23.1 represents a coupling of this kind between two common emitter stages.

An RC connection allows ac, but blocks the dc between the two stages, making them independent as far as the dc bias setting is concerned. The operation point can be determined separately, for each single stage.

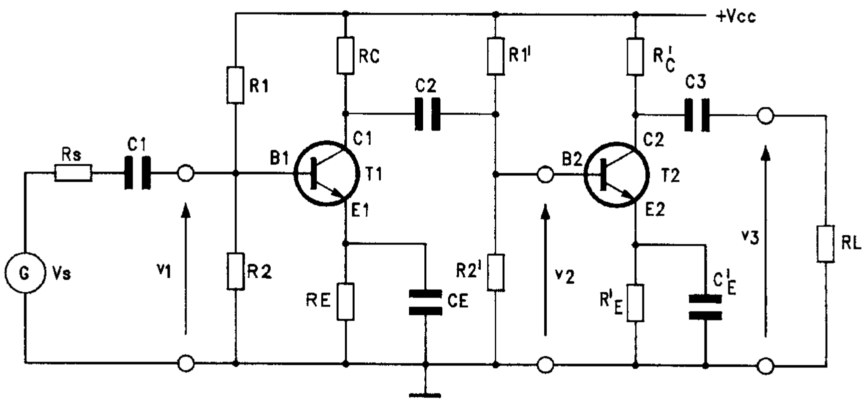


fig.B23.1

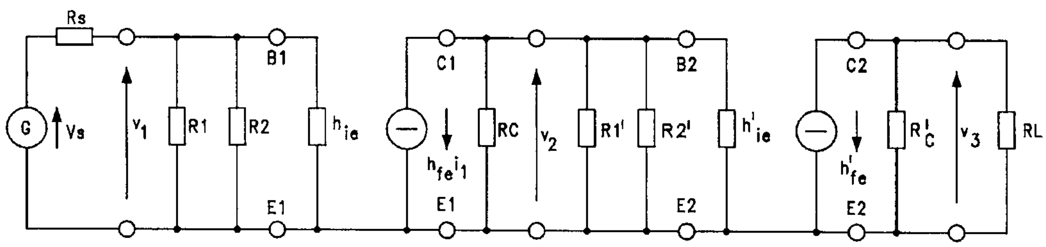


fig. B23.2

Characteristics as function of the h parameters

An ac or dynamic study of the amplifier of figure B23.1 is carried out using the equivalent circuits of each single stage. The diagram of the figure B23.1 becomes the one of figure B23.2. In the circuit there are some simplifications, i.e. the parameters h_{re} and h_{oe} of both transistors are assumed negligible.

Analysis of the equivalent circuit enables the calculation of the following dynamic characteristics:

1. *Total input resistance R_{it}*

   $R_{it} = v_1 / i_{1t} = R1//R2//h_{ie}$

2. *Voltage gains A_{v1} and A_{v2}*

   $A_{v1} = v_2 / v_1 = -h_{fe} \cdot (Rc//R'_{it})/h_{ie}$

   where $R'_{it} = R'_1//R'_2//h'_{ie}$

   $A_{v2} = v_3 / v_2 = -h'_{fe} \cdot (R'c//R_L)/h'_{ie}$

3. *Voltage gain A_{v12}*

   $A_{v12} = A_{v1} \cdot A_{v2}$

4. *Total voltage gain A_{vt}*

   the generator has an internal resistance which causes a voltage drop across it, when supplying current to the circuit. The signal attenuation is :

   $\alpha = v_1 / v_s = R_{it} / (R_s + R_{it})$

   The total voltage gain is:

   $A_{vt} = v_3 / v_s = \alpha \cdot A_{v12}$

B23.2 EXERCISES

➲ *MCM5*	**Disconnect all jumpers** **Set in OFF all S switches**
➲ *SIS1*	**Turn all switches *OFF***
➲ *SIS2*	**Insert lesson code: B23**

- Insert jumpers J2, J5, J6, J11, J17, J26, J34, J36, J40, J44 and connect the instruments to produce the circuit of figure B23.3.

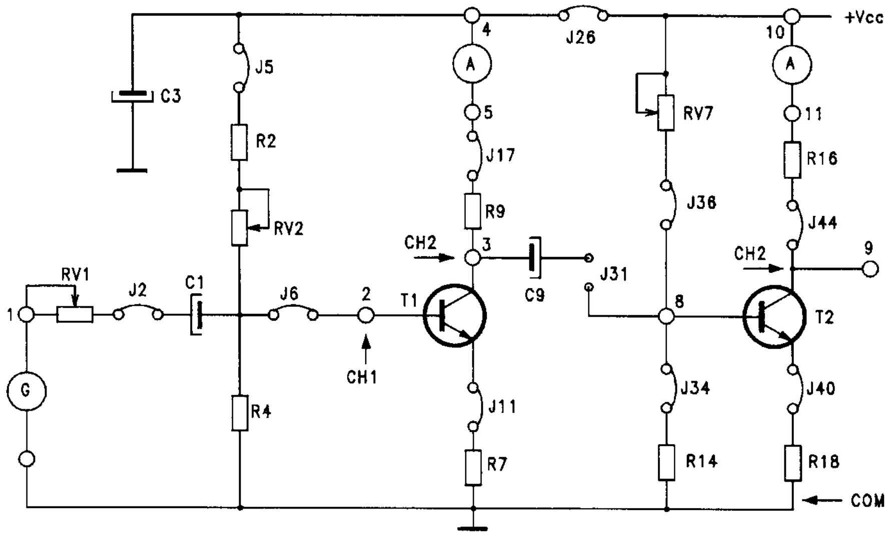


fig. B23.3

- Set Vcc adjustable power supply to 20V and adjust RV1 to mid-position
- rotate RV2 and RV7 to obtain: $I_{CQ1} \approx 10$ mA, $I_{CQ2} \approx 20$ mA
- Insert jumper J31

Q1 *What is the configuration of the two stages in fig B23.2?*

SET

A	*B*	
1	5	common emitter
2	3	common base
3	1	dual load
4	2	emitter follower
5	4	common collector

- Connect the oscilloscope channel 1 at terminal 2 (input signal) and the channel 2 at terminal 3 (first stage output signal).
- Connect the function generator at terminals 1 and ground with a sine wave, 1 KHz and vary the amplitude value to check 200 mVpp at terminal 2.

- determine the voltage gain and the phase shift between the two signals
- move the oscilloscope channel 2 at terminal 9 (second stage output signal)
- Check the phase differences between the input signal and the output signals across the two stages

Q2 *What is the total gain of the circuit, and what is the phase shift between the input signal and the output?*

SET A	SET B		
1	3	$A_{vt} = A_{v1} + A_{v2}$	shift = 45°
2	5	$A_{vt} = A_{v1} \cdot A_{v2}$	shift = 45°
3	1	$A_{vt} = A_{v1} \cdot A_{v2}$	shift = 90°
4	2	$A_{vt} = A_{v1} + A_{v2}$	shift = 180°
5	4	$A_{vt} = A_{v1} \cdot A_{v2}$	shift = 0°

B23.3 SUMMARY QUESTIONS

Q3 *Why are amplifiers with more than one stage needed?*

SET A	SET B	
1	4	to increase the operating frequency
2	1	to match the source to the load
3	5	to obtain a high input resistance
4	3	to diminish the signal distortion
5	2	to obtain all the above advantages

Q4 *The characteristics of an amplifier with several stages depend on:*

SET A	SET B	
1	2	the characteristics of the first stage
2	5	the characteristics of the last stage
3	4	the characteristics of each stage
4	3	the load
5	1	the power supply voltage

Q5 *An amplifier with several stages:*

SET		
A	*B*	
1	3	can be composed of different stages
2	4	must be composed of similar stages
3	5	must be composed of different stages
4	1	has a first stage with a dual load
5	2	has a follower stage across the output

Q6 *In a multi-stage amplifier, consisting of two common emitter stages, what is the phase shift between the input and the output signals?*

SET		
A	*B*	
1	2	0 degrees
2	5	90 degrees
3	1	45 degrees
4	3	180 degrees
5	4	270 degrees

Q7 *RC coupling, in amplifiers with several stages, allows you to:*

SET		
A	*B*	
1	6	bias the second stage properly
2	1	send the ac component af a signal from one stage to the next, without affecting the bias
3	4	obtain an oscillating signal
4	3	electrically isolate the different stages fromeach other
5	2	increase the output power of the amplifier
6	5	upgrade the frequency answer at high frequencies

Lesson B24: TRANSFORMER COUPLING

OBJECTIVES

- Study of a 2-stage circuit amplifier with transformer coupling:
  - measurement of the voltage gains
  - use of an RC network to obtain a better frequency response of the amplifier

EQUIPMENT REQUIRED

- base unit for the IPES system (power supply mod. PS1-PSU/EV, module holder structure for modules mod. MU/EV), individual control unit mod. SIS1/SIS2/SIS3
- experiment module mod. MCM5/ EV
- function generator
- oscilloscope
- multimeter.

B24.1 BASIC THEORY

In this case the link between two amplifier stages is achieved using a transformer. The figure B24.1 shows a typical coupling between two dual-load transistor amplifiers.

As you can note from figure B24.1 the primary of the transformer replaces the usual load resistance R_L. As the transformer behaves like an inductance (which has zero or very low resistance), the dc (or Quiescent) current I_{CQ} across the first stage does not dissipate power as a resistance would. As for ac components, the dynamic load is that of the secondary (R) seen from the primary, and is equal to $n^2 \cdot R$, where $\boldsymbol{n}$ is the transform ratio of the transformer. As far as the the dc bias is concerned, the transformer makes the two stages independent of each other. The Q or bias point can be determined separately for each stage.

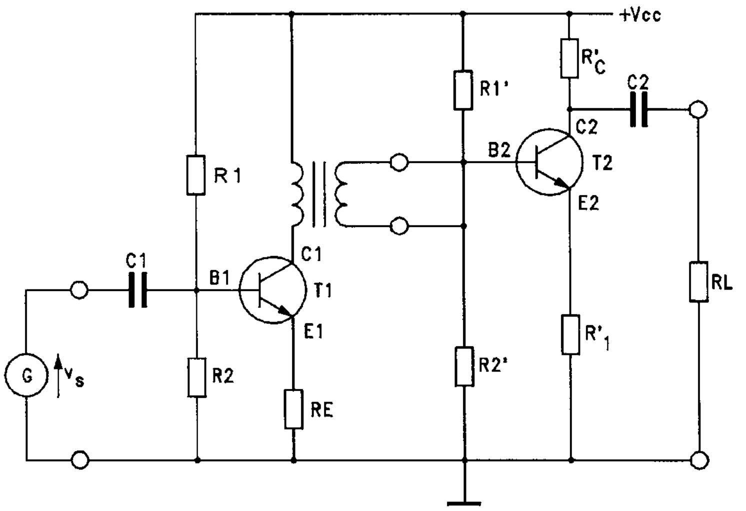


fig.B24.1

The transformer system can also be used in the coupling between final stage and the load in the power amplifiers (figure B24.2). In this case the transformer is called the "output transformer".

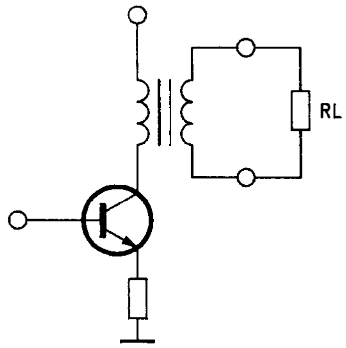


fig.B24.2

The advantages of the transformer coupling are: absence of d.c. current through the load and higher power efficiency.

The disadvantages are: larger volume and weight of the transformer, frequency limitations of the transformer and non linearity of the response curve.

Because of these disadvantages, the use of the transformer in low-frequency, small signals amplifiers is not recommended. On the contrary, it is widely applied in high-frequency tuned amplifiers, where the transformer is used to realize resonant circuits.

In an amplifier using transformers, the a.c. component in the primary depends on the reactance of the winding. The amplification is proportional to the reactance of the transformer so the output signal depends on the frequency. To limit this problem, an RC circuit can be used in parallel to the primary (figure B24.3).

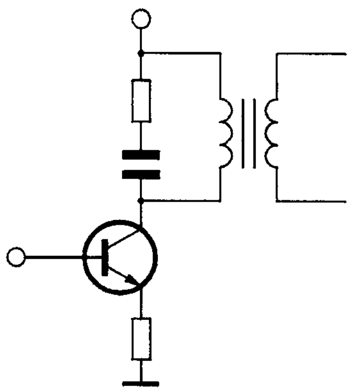


fig. B24.3

Biasing

In the study of the circuit, two load lines are defined: a static and a dynamic one. The static load line is almost vertical, because the resistance of the transformer primary is very small. In absence of signal the collector voltage is practically equal to Vcc.

The dynamic load line has a slope equal to: $-1/(n^2 \cdot R_L)$ where ***n*** is the turns or transform ratio of the transformer.

Characteristics as function of the h parameters

Using simplified equivalent circuits, the two-stage amplifier of figure B24.1 becomes as shown in figure B24.4.

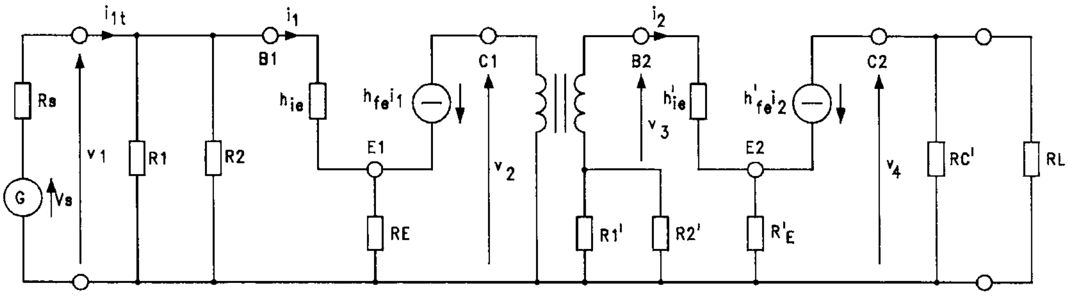


fig. B24.4

An analysis of the equivalent circuit enables the calculation of the following dynamic characteristics:

1. *Total input resistance Rit*

   $Rit = v_1/i_{1t} = R1//R2//Ri$, where $Ri = h_{ie} + h_{fe} \cdot R_E$

2. *Voltage gain of the second stage A_{v2}*

   $$A_{v2} = \frac{v_4}{v_3} = -\frac{h'_{fe} \cdot (R'_c // R_L)}{h'_{ie} + R'_B + R'_E \cdot h'_{fe}}$$
   where $R'_B = R'_1//R'_2$

3. *Voltage gain of the transformer A_{vtr}*

   $A_{vtr} = v_3 / v_2 = 1/n$, where ***n*** is the transform ratio

4. *Voltage gain of the first stage A_{v1}*

   $$A_{v1} = \frac{v_2}{v_1} = -\frac{h_{fe} \cdot Rp)}{h_{ie} + R_E \cdot h_{fe}}$$

   where $Rp = n^2 \cdot R'_i$; $R'_i = h'_{ie} + R'_B + h_{fe} \cdot R'_E$

5. *Voltage gain A_{v12}*: $A_{v12} = A_{v1} \cdot A_{vtr} \cdot A_{v2}$

6. *Total voltage gain A_{vt}*: $A_{vt} = v_4 / v_s = \alpha \cdot A_{v12}$

   with: $\alpha = v_1 / v_s = Ri / (Rs + Ri)$

B24.2 EXERCISES

➲ *MCM5*	**Disconnect all jumpers** **Set in OFF all S switches**
➲ *SIS1*	**Turn all switches *OFF***
➲ *SIS2*	**Insert lesson code: B24**

- Insert jumpers J2, J5, J6, J11, J20, J21, J25, J26, J27, J40, J44 and the instruments to Produce the circuit of figure B24.5.

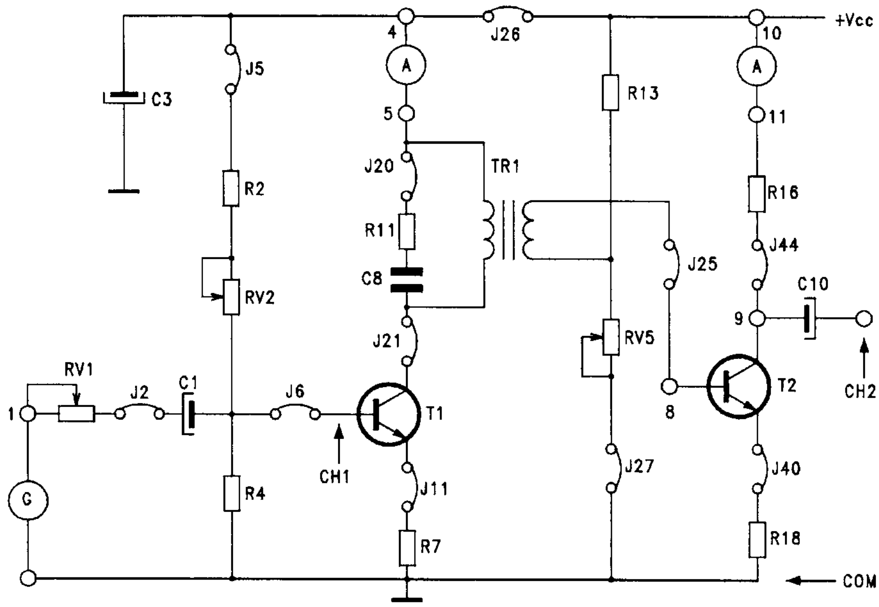


fig. B24.5

- Set Vcc adjustable power supply to 20V and adjust RV1 to mid position.
- Vary RV2 and RV5 to obtain: $I_{CQ1} \approx 10$ mA, $I_{CQ2} \approx 10$ mA
- For the next calculations, remember that the transformer has 350 turns on the primary and 700 on the secondary, so $n = 350/700 = 0.5$
- Connect the oscilloscope channel 1 at terminal 2 (input signal) and channel 2 at terminal 9 (output signal).
- Connect the function generator at terminals 1 and ground with a sine wave, 1 KHz and vary the amplitude value to check 100 mVpp at terminal 2.
- Measure the output signal; calculate the total voltage gain of the amplifier.
- Without change the input signal parameters, measure at terminal 8 the amplitude of the transformer output signal; calculate the gain across the second stage.
- vary the input signal frequency and note how amplification changes.
- disconnect the series components R11-C8 from the transformer primary, by removing J20. Vary the input frequency and again observe the changes in the gain.

Q1 *What are the advantages of connecting the RC network to the primary of the transformer?*

SET		
A	*B*	
1	5	more constant gain and less distortion, as the operating frequency varies
2	3	reduction of the output impedance
3	1	none
4	2	the power dissipated is reduced
5	4	higher amplification

➲ *SIS1*	**Turn switch SW9 *ON***
➲ *SIS2*	**Press *INS***

Q2 *What is the reason for the malfunction in the circuit?*

SET		
A	*B*	
1	4	the resistance R18 has changed
2	1	the still point of T1 has changed
3	2	the base of T2 has been connected to ground
4	3	the turns ratio of the transformer has been changed

➲ *SIS1*	**Turn switch SW9 *OFF***

➲ *SIS1*	**Turn switch SW1 *ON***
➲ *SIS2*	**Press *INS***

Q3 *What is the reason for the circuit malfunction?*

SET		
A	*B*	
1	2	the collector and emitter of T2 are short circuited
2	4	the base of T2 is not properly biased because RV5 is short circuited
3	1	the base of T2 is not biased properly because the secondary of the transformer is disconnected
4	5	emitter and base of the transistor T1 are short-circuited
5	3	the power supply Vcc is missing

➲ *SIS1*	**Turn SW1 *OFF***

B24.3 SUMMARY QUESTIONS

Q4 *Using a transformer in place of the collector resistance will:*

SET

A	*B*	
1	4	dissipate more d.c.power
2	1	dissipate less d.c power
3	5	dissipate less a.c. power
4	2	supply more a.c. power to the load
5	3	amplify d.c. signals

Q5 *The transformer coupling in amplifiers with several stages, allows you to:*

SET

A	*B*	
1	6	bias the second stage properly
2	4	send the a.c. component of the signal from one stage to the next without changing bias settings
3	1	obtain an oscillating signal
4	2	electrically isolate the different stages from each other
5	3	increase the power at the amplifier output
6	5	improve the response curve especially at high frequencies

Q6 *Transformer coupling is used:*

SET

A	*B*	
1	4	in d.c. current amplifiers
2	3	in multi-stage amplifiers and for coupling to the generator
3	2	in self-oscillating amplifiers
4	1	in multi-stage amplifiers and for coupling to the load

Lesson B25: DIRECT COUPLING

OBJECTIVES

- Study of a circuit amplifier with two stages and direct coupling:
- calculation of the voltage gain of each stage
- calculation of the total gain of the amplifier
- measurement of the voltage gains
- determination of the phase difference between input signal and output signals

EQUIPMENT REQUIRED

- base unit for the IPES system (power supply mod. PS1-PSU/EV, module holder structure for modules mod. MU/EV), individual control unit mod. SIS1/SIS2/SIS3
- experiment module mod. MCM5/ EV
- function generator
- oscilloscope
- multimeter.

B25.1 BASIC THEORY

Direct coupling between stages does not have interposed capacitances nor transformers, i..e. it does not use devices which separate the d.c. voltages needed for biasing. The figure B25.1 shows an example of direct coupling between two transistor stages, a dual-load and a common collector one.

Frequency response with direct coupling extends from the d.c. to the cut-off frequency determined by the different stages composing the amplifier. The direct coupling is also called "d.c.".

The worst disadvantages of the direct connection is determined by the fact that the d.c. voltages of the two stages are not independent. A shift of the Q point of the first stage will change the Q point of the second circuit.

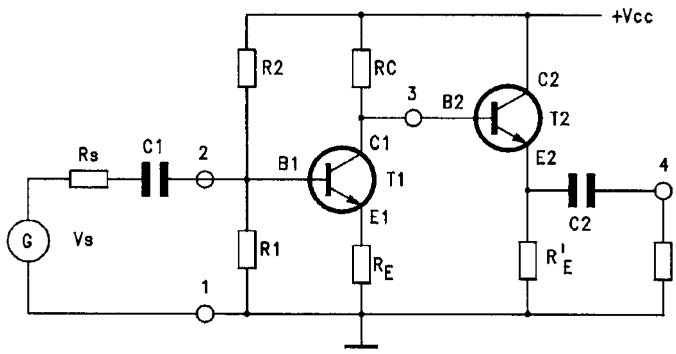


fig.B25.1

Characteristics as function of the h parameters

Using simplified equivalent circuits for the transistor, the diagram of figure B25.1 becomes the one of fig.B25.2.

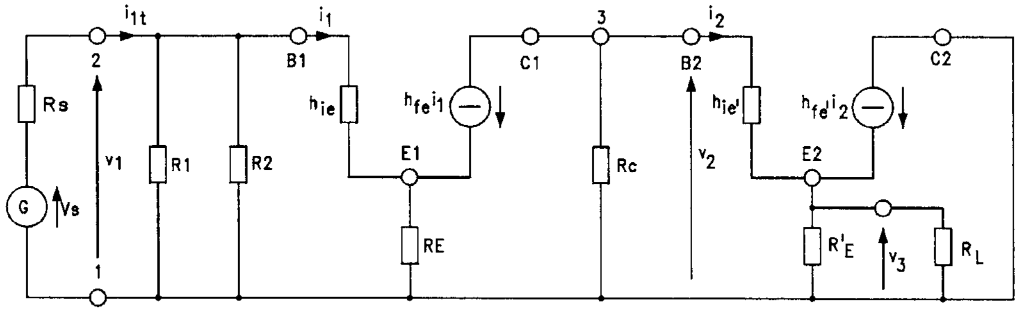


fig. B25.2

The study of the equivalent circuit enables the calculation of the dynamic characteristics:

1. *Total input resistance Rit*

   $Rit = v_1 / i_{1t} = R1 \,//\, R2 \,//\, Ri$

   where $Ri = h_{ie} + R_E \cdot h_{fe}$

2. *Voltage gains A_{v1} and A_{v2}*

   $$A_{v1} = \frac{v2}{v1} = -\frac{h_{fe} \cdot (Rc//R'i)}{h_{ie} + R_E \cdot h_{fe}}$$

   $A_{v2} = v_3 / v_2 = h'_{fe} \cdot (R_L//R'_E)/R'i$

   where $R'i = h'_{ie} + h'_{fe} \cdot (R_L//R'_E)$

3. *Voltage gain A_{v12}*

   $A_{v12} = A_{v1} \cdot A_{v2}$

4. *Total voltage gain A_{vc}*

   $A_{vc} = v_3 / v_s = \alpha \cdot A_{v12}$

   with: $\alpha = v_1 / v_s = Rit / (Rs + Rit)$

B25.2 EXERCISES

➲ *MCM5*	**Disconnect all jumpers** **Set in OFF all S switches**
➲ *SIS1*	**Turn all switches *OFF***
➲ *SIS2*	**Insert lesson code: B25**

- Insert jumpers J2, J5, J6, J11, J17, J26, J29, J42, J46 and the instruments to produce the circuit of fig.B25.3.

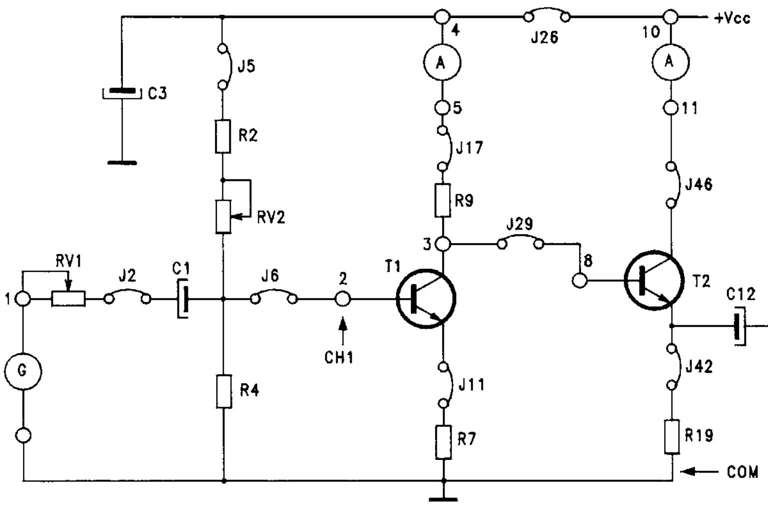


fig. B25.3

- Set Vcc = 20 V (variable power supply) and adjust RV1 to mid position.
- Vary RV2 to obtain $I_{CQ1} \approx 10$ mA
- Measure V_{CEQ1}, V_{CEQ2}, I_{CQ2}
- Analyze the way the operating points vary, as trimmer RV2 is varied

Q1 *An increase of I_{CQ1} causes:*

SET

A	*B*	
1	2	an increase of V_{CEQ1}, decrease of I_{CQ2}, increase of V_{CEQ2}
2	3	decrease of V_{CEQ1}, decrease of I_{CQ2}, increase of V_{CEQ2}
3	4	increase of V_{BEQ1}, increase of I_{CQ2}, increase of V_{CEQ2}
4	1	decrease of V_{CEQ1}, decrease of I_{CQ2}, decrease of V_{CEQ2}

- take the Q point back to normal.
- Connect the oscilloscope channel 1 at terminal 2 (input signal) and channel 2 at terminal 12 (output signal).
- Connect the function generator at terminals 1 and ground with a sine wave, 1 KHz and vary the amplitude value to check 200 mVpp at terminal 2.
- Measure the output voltage amplitude at trminal 12, and calculate the voltage gain of the circuit.
- measure the phase shift introduced by the circuit

Q2 *What is the phase shift, and what causes it?*

SET		
A	*B*	
1	5	shift = 0°, due to both stages
2	3	shift = 45°, due to the first stage
3	1	shift =180°, due to the second stage
4	2	shift =180°, due to the first stage
5	4	shift =180°, due to a shift of 90° of both stages

B25.3 SUMMARY QUESTIONS

Q3 *Direct coupling is used when an amplifier is required to amplify:*

SET		
A	*B*	
1	3	high frequency signals
2	5	low frequency signals
3	4	alternating signals
4	1	signals containing a d.c. component
5	2	periodic signals

Q4 *In amplifiers with direct coupling:*

SET		
A	*B*	
1	4	the bias currents and voltages of one stage do not affect those of another
2	1	only the bias currents of one stage affect those of another stage
3	2	the bias currents and voltages of one stage can affect those of another
4	3	the first stage must not be biased

Lesson B26: DARLINGTON CONNECTION

OBJECTIVES

- Examination of the operating characteristics of a Darlington connection

EQUIPMENT REQUIRED

- base unit for the IPES system (power supply mod. PS1-PSU/EV, module holder structure for modules mod. MU/EV), individual control unit mod. SIS1/SIS2/SIS3
- experiment module mod. MCM5/ EV
- function generator
- oscilloscope
- multimeter.

B26.1 BASIC THEORY

Two transistors are in Darlington connection, (or make a Darlington pair) when the emitter current of the first is also the base current of the second (fig.B26.1).

A Darlington pair produces a high current gain amplifier with a high input resistance. It is often used in the emitter follower circuit (figure B26.2).

Often the transistor manufacturers place the Darlington pair into a single case. This has the electrical advantage of keeping both transistors at the same operating temperature.

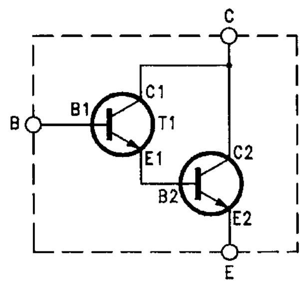


fig.B26.1

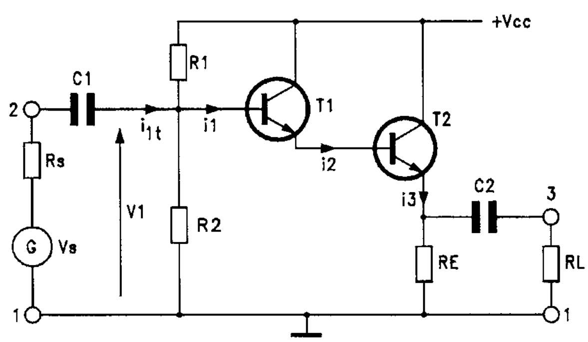


fig.B26.2

Characteristics as function of the h parameters

The two transistors of a Darlington connection can be considered equivalent to a single transistor characterized by the following h parameters:

$h_{fe} = h_{fe1} + h_{fe2} \cdot (1 + h_{fe1})$
$h_{ie} = h_{ie1} + h_{ie2} \cdot (1 + h_{fe1})$

As $h_{fe1} >> 1$ and $h_{fe2} >> 1$, the following simplified relations can be used:

$h_{fe} = h_{fe1} \cdot h_{fe2}$
$h_{ie} = h_{ie1} + (h_{ie2} \cdot h_{fe1})$
$h_{re} = h_{ie2} \cdot h_{oe1}$
$h_{oe} = h_{oe2} + h_{oe1} \cdot h_{fe2}$

Using the last formula, a Darlington pair can be considered as a single transistor. In the example of an emitter follower of figure B26.2 the following approximate relations apply:

1. *Current gain Ai*

$$A_i = \frac{i_3}{i_1} = \frac{h_{fe1} \cdot h_{fe2}}{1 + (h_{oe2} + h_{fe2} \cdot h_{oe1}) \cdot R_p}$$

where $Rp = R_E // R_L$

2. *Input resistance Rit*

$Rit = v_1 / i_{1t} = R1 // R2 // Ri$

where $Ri = h_{ie1} + h_{fe1} \cdot h_{ie2} + Rp \cdot Ai$

3. *Voltage gain Av*

$Av = v_2 / v_1 = 1 - [h_{ie1} + (h_{fe1} \cdot h_{ie2})]/Ri$

4. *Output resistance Ro*

$$\frac{1}{R_o} = \frac{1}{R_p} + h_{oe2} + (h_{oe1} \cdot hfe2) + \frac{1 + h_{fe1} \cdot h_{fe2}}{h_{ie1} + (h_{fe1} \cdot h_{ie2}) + R_{eq}}$$

with Req=R1//R2//Rs, and Rs internal resistance of the generator

The features of an emitter follower with Darlington connection compared to a normal one (with a single transistor) are:
- higher input resistance Ri
- higher current gain Ai
- voltage gain Av more close to 1
- smaller output resistance Ro

B26.2 EXERCISES

➲ *MCM5*	**Disconnect all jumpers** **Set in OFF all S switches**
➲ *SIS1*	**Turn all switches *OFF***
➲ *SIS2*	**Insert lesson code: B26**

D.c. gain

- Insert jumpers J5, J8, J15, J19, J26, J33, J40, J46, and the instruments to produce the circuit of fig.B26.3.

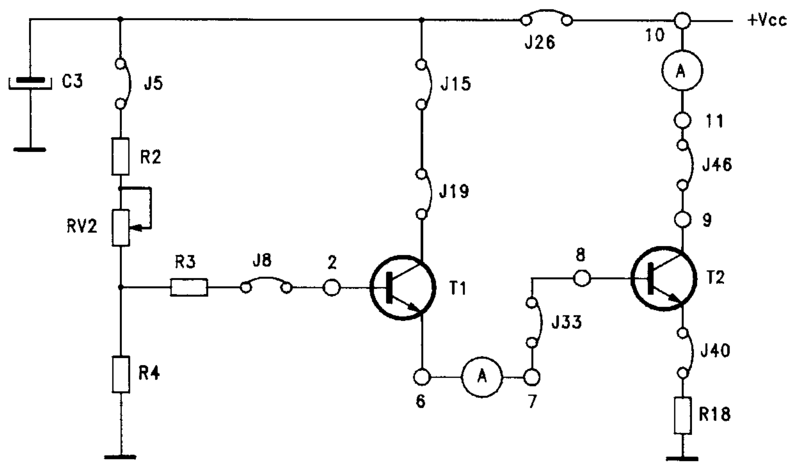


fig.B26.3

- Set Vcc adjustable power supply to 20V and vary RV2 to obtain a current $I_{CQ2} \approx 30$ mA
- measure the base current of transistor T2
- measure the voltage present across the resistance R3
- calculate the base current of transistor T1
- as the base current of transistor T2 is almost equal to the collector current of the transistor T1, calculate the d.c. current gains of each transistor, and calculate the total current gain of the Darlington pair

Q1 *The two current gains h_{FE} are:*

SET

A	*B*	
1	5	equal, but less than 20
2	3	h_{FE2} is 1, while h_{FE1} is very high
3	4	h_{FE1} is very low, while h_{FE2} is very high
4	1	equal, but depend on voltage Vcc
5	2	different, but both higher than 100

Measurement of the saturation voltage

- Remove all jumpers, insert J5, J6, J17, J22, J26, J33, J35, J39, and the instruments to produce the circuit of figure B26.4.

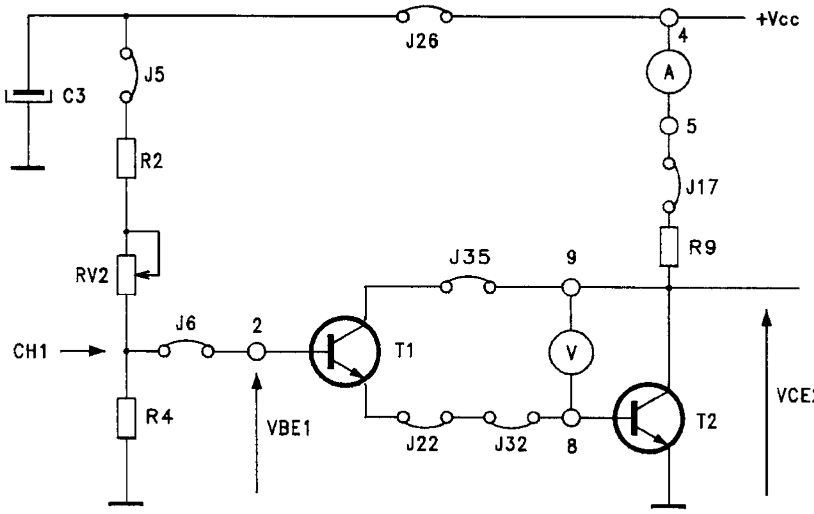


fig.B26.4

- Adjust RV2 until the voltage V_{CB1} becomes negative (T1 into saturation), so to take the Darlington circuit itself into saturation
- measure V_{CE1sat} and V_{BE2}

Q2 *What is the relationship of the Darlington saturation voltages?*

SET

A	*B*	
1	4	$V_{CEsat} = V_{CE1sat} + V_{CE2sat}$
2	1	$V_{CEsat} = V_{CE1sat}$
3	5	$V_{CEsat} = V_{CE1sat} + V_{CB2}$
4	2	$V_{CEsat} = V_{BE1sat}$
5	3	$V_{CEsat} = V_{BE2} + V_{CE1sat}$

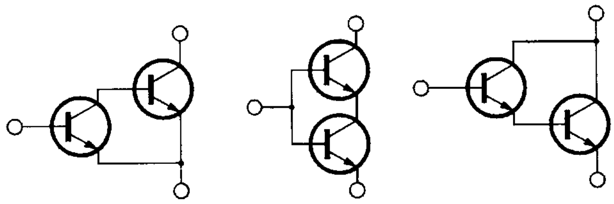
The saturation voltage V_{CEsat} of a Darlington connection is greater than the saturation voltage of a single transistor, since it is equal to the collector-emitter voltage V_{CE2} of the transistor T2, which cannot be taken into saturation.

B26.3 SUMMARY QUESTIONS

Q3 *Which of the following connections represents a Darlington circuit?*

SET

A	*B*	



a) b) c)

A	*B*	
1	3	a and b
2	1	c
3	5	a
4	6	b
5	4	a and c
6	2	b and c

Q4 *The d.c. current gain of a Darlington pair, with two transistors of gains h_{FE1} and h_{FE2}, is equal to:*

SET

A	*B*	
1	2	$1/(h_{FE1} \cdot h_{FE2})$
2	4	$h_{FE1} \cdot h_{FE2}$
3	5	$h_{FE1} + h_{FE2}$
4	3	$h_{FE1} \cdot h_{FE2}/2$
5	1	$(h_{FE1} + h_{FE2})/2$

Q5 *Compared to a single transistor, the Darlington connection has:*

SET

A	*B*	
1	4	a lower input resistance
2	5	a higher output resistance
3	1	a higher input resistance and a higher current gain
4	2	a reduction of the current gain
5	3	a wider pass band with better frequency response

Lesson B27: CASCODE and BOOTSTRAP CONNECTIONS

OBJECTIVES

- Study of the Cascode amplifier
- measurement of the voltage gain Av
- measurement of the higher cut-off frequency of a Cascode circuit
- Study of a Bootstrap connection in an emitter follower circuit
- measurement of the input resistance with and without Bootstrap connection

EQUIPMENT REQUIRED

- base unit for the IPES system (power supply mod. PS1-PSU/EV, module holder structure for modules mod. MU/EV), individual control unit mod. SIS1/SIS2/SIS3
- experiment module mod. MCM5/ EV
- function generator
- oscilloscope
- multimeter.

B27.1 BASIC THEORY

Cascode Amplifier

The Cascode amplifier is a multi-stage amplifier with direct coupling. It consists of a common emitter transistor with a common base transistor in cascade (figure B27.1).

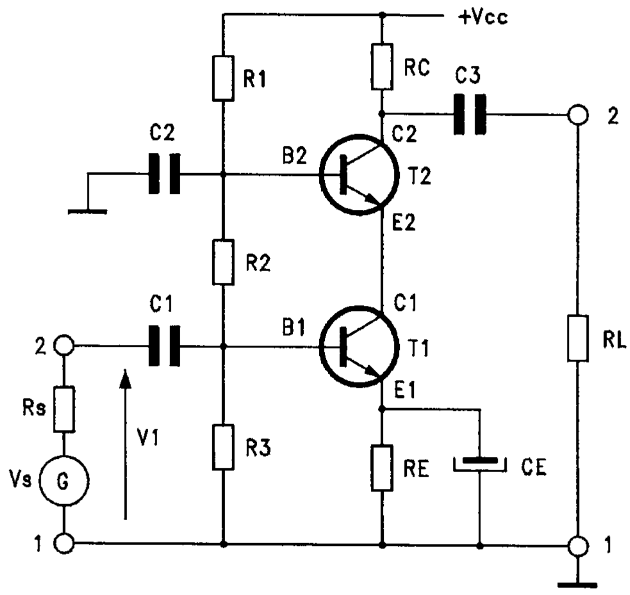


fig.B27.1

This circuit provides:

- very high output resistance, similar to a common base circuit
- high stability and frequency response.

These characteristics make the Cascode connection particularly useful at high frequency.

Cascode: characteristics as function of the h parameters

Using the equivalent transistor circuit, and taking h_{re}, h_{oe}, h_{rb}, h_{ob} as negligible, the circuit of figure B27.1 can be represented as in figure B27.2.

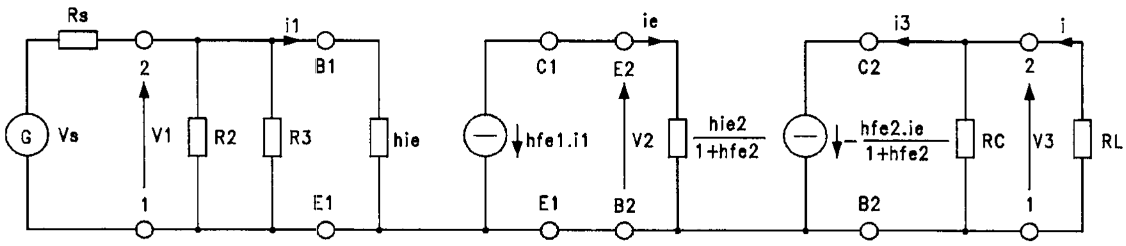


fig. B27.2

At low frequency the Cascode has the following characteristics:

1. *Current gain Ai*

   $Ai = i_3 / i_1 = h_{fe1}$

2. *Input resistance Rit*

   $Rit = v_1 / i_1 = R2//R3//Ri$

   where $Ri = h_{ie1}$

3. *Voltage gain Av*

   $Av = v_3 / v_1 = -Rp \cdot h_{fe1} / h_{ie1}$

   where $Rp = Rc // R_L$

4. *Output resistance Ro*

   $Ro = v_3 / i_3 \approx h_{fe2} / h_{oe2}$

Bootstrap effect biasing

The input resistance of the amplifier depends much on the base biasing resistance R_B. Since, for good stability R_B cannot be too high, a Bootstrap connection is used to obtain high input resistance values, but maintaining a low base resistance value. The figure B27.3a shows a biased emitter follower with Bootstrap connection.

From a dynamic viewpoint, i.e. considering only the ac signal components, the circuit becomes the one of fig.B27.3b.

If the input signal (on the Base) increases, at the same time the output signal increases (on the Emitter), as the voltage gain of a follower is almost equal to one. The current across R3 is then much smaller than would be the case if R3 were connected directly to ground: it follows that the equivalent resistance of the input circuit is much higher than R3.

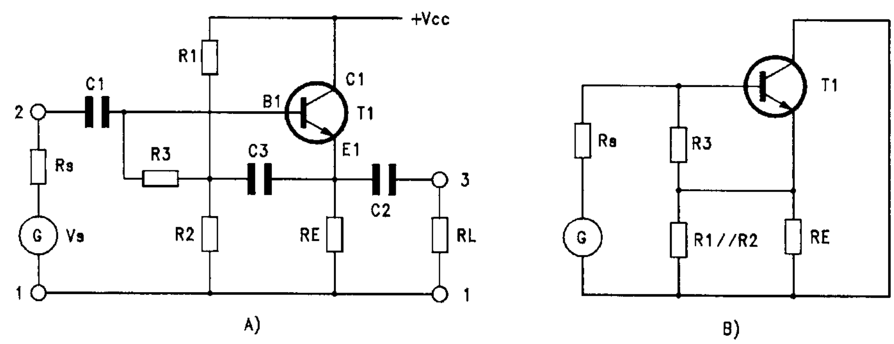


fig.B27.3

Bootstrap: characteristics as function of the h parameters

Considering h_{re} as negligible, the equivalent small signal circuit to is as shown in figure B27.4. Note that the resistance R3, to which the Miller theorem has been applied, has been divided into two parts, one connected to the input (R') and the other to the emitter (R").

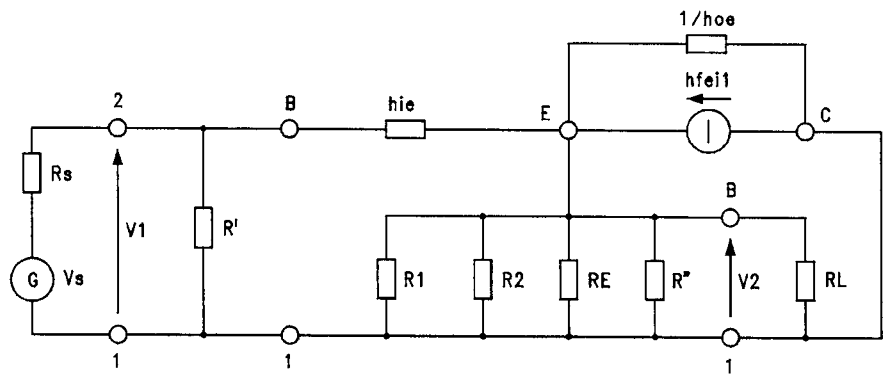


fig. B27.4

The Bootstrap circuit has the following characteristics:

1. *Input resistance Ri*

   $Ri = v_1 / i_1 = h_{ie} + (1 + h_{fe}) \cdot Rp$

   where $Rp = R_E \,//\, R1 \,//\, R2 \,//\, R_L$

2. *Voltage gain Av*

   $Av = v_2 / v_1 = 1 - h_{ie} / Ri$

3. *Total input resistance Rit*

   $Rit = v_1 / i_{1t} = R' \,//\, Ri$

   where $R' = R3 / (1 - Av)$

   NOTE: These relations are true if the absolute value of R", equal to $[Av \cdot R3/(Av - 1)]$, is much bigger than R_E.

4. *Total voltage gain Avt*

   $Avt = v_2 / v_s = \alpha \cdot Av$

   where $\alpha = v_1 / v_s = Rit / (Rs + Rit)$

B27.2 EXERCISES

➲ *MCM5*	**Disconnect all jumpers** **Set in OFF all S switches**
➲ *SIS1*	**Turn all switches *OFF***
➲ *SIS2*	**Insert lesson code: B27**

Cascode circuit

- Insert jumpers J2, J5, J6, J11, J13, J24, J36, J37, J44 and the instruments to produce the circuit of fig.B27.5.

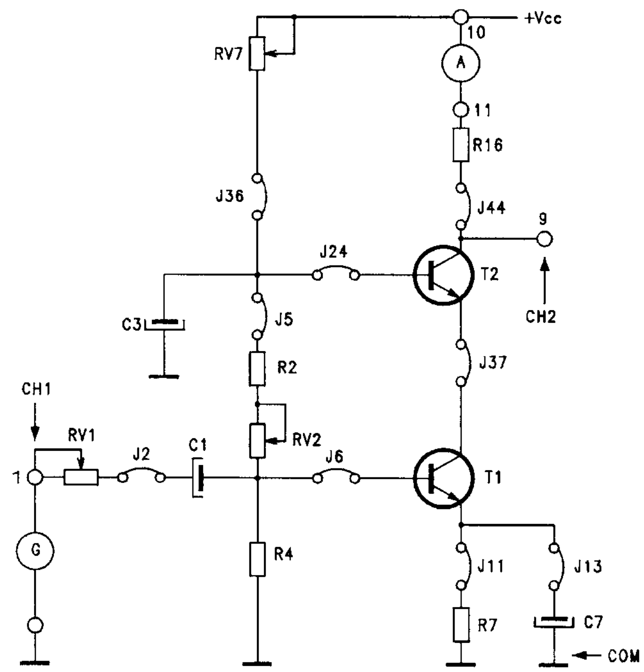


fig.B27.5

- Set Vcc adjustable power supply to 20V and adjust RV1 to mid position.
- Vary RV2 completely C.C.W. (lowest resistance) and adjust RV7 to obtain a collector current of about 10 mA.
- Connect the oscilloscope channel 1 at terminal 2 (input signal) and the channel 2 at terminal 9 (output signal).
- Connect the function generator at terminals 1 and ground with a sine wave, 1 KHz and vary the amplitude value to check 40 mVpp at terminal 2.
- if the wave-form is distorted, adjust RV1, to reduce it
- measure the output voltage and calculate the voltage gain of the amplifier

Q1 *What is the voltage gain ?*

SET

A	*B*	
1	4	about 120
2	5	about 1
3	2	about 12
4	3	about 640
5	1	about 1200

- Vary the input frequency to measure the upper cut-off frequency of the amplifier.

Remind that the cut-off frequencies are defined as the frequencies at which the output signal drops by 3 dB compared to the maximum value. In other words at the cut-off frequencies the signal is equal to $1/\sqrt{2}$, of the max. value.

- Recreate the common emitter circuit of figure B20.12: remove all jumpers, insert J2, J5, J6, J11, J13, J17, J26 and measure the upper cut-off frequency with this method.

Q2 *From the comparison of the cut-off frequencies of the two circuits we can say that:*

SET

A	*B*	
1	2	the Cascode cut-off frequency is higher
2	4	they are almost equal
3	1	the common emitter one is slightly higher
4	5	the common emitter one is much higher
5	3	the Cascode one is 100 times higher

Bootstrap connection

- Remove all jumpers, insert J1, J2, J5, J7, J9, J12, J19, J26 and instruments to produce the circuit of fig.B27.6

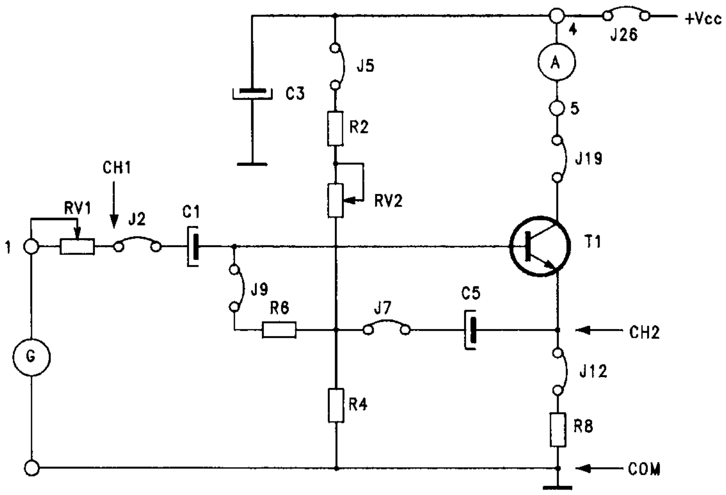


fig.B27.6

- Keep the Vcc variable supply to 20 V and adjust RV2 to obtain a current I_{CQ} of 4.5 mA
- Vary RV1 completely C.W. (minimum resistance).
- Connect the oscilloscope channel 1 at terminal 2 (input signal) and the channel 2 at terminal 6 (output signal).

- Connect the function generator at terminals 1 and ground with a sine wave, 1 KHz and vary the amplitude value to check 4 Vpp at terminal 2.
- display on the oscilloscope the input and output voltages of the circuit
- remove jumper J1, to add trimmer RV1 in series with the input of the amplifier
- adjusting trimmer RV1, use the method of reducing the input voltage to half (see lesson B20) to measure the total input resistance Rit of the amplifier

Q3 *What is the approximate measured value of resistance Rit?*

SET

A	*B*	
1	3	a few ohms
2	5	a few hundred ohms
3	1	1 kΩ
4	2	10 kΩ
5	6	23 KΩ
6	4	more than 50 KΩ

- Remove jumpers J7, J9, insert J1, J6 (the circuit configuration is then one of a standard emitter follower).
- repeat the last measurement of the input resistance Rit of the circuit.

Q4 *From the comparison between the two measured input resistances, you can say that the Bootstrap connection :*

SET

A	*B*	
1	4	noticeably reduces the input resistance of the amplifier
2	1	reduces the power supply voltage
3	2	noticeable increases the input resistance of the circuit
4	5	reduces the load resistance
5	3	noticeably reduces the high frequency disturbances on the load

B27.3 SUMMARY QUESTIONS

Q5 *How many active devices does a Cascode amplifier have?*

SET

A	*B*	
1	3	one transistor
2	6	two transistors
3	1	three transistors
4	5	two transistors and an SCR
5	4	three transistors and 1 Mosfet Depletion
6	2	one transistor and three diodes

Q6 *What are the advantages of a Cascode amplifier ?*

SET

A	*B*	
1	2	reduction of the band width and increase of the
2	1	increase of the upper cut-off frequency compared to a single transistor amplifier
3	5	better matching between source and load
4	3	increases the output signal frequency compared to the input one
5	4	maintenance of the phase relations between input signal and output signal

Q7 *Consider an emitter follower with Bootstrap connection with the following values:*

R1 = 100 KΩ   R2 = 33 KΩ R_L = 10 KΩ R_E = 1 KΩ
h_{ie} = 1 KΩ h_{fe} = 100   R3 = 56 KΩ.

What is the total input resistance Rit?

SET

A	*B*	
1	6	560 Ω
2	3	89.6KΩ
3	4	678 KΩ
4	1	5.6 Ω
5	2	1 KΩ
6	5	10 KΩ

Lesson B28: DIFFERENTIAL AMPLIFIER

OBJECTIVES

- To become familiar with the characteristics of the differential amplifier
- Measurement of the gain in differential mode
- Measurement of the common mode gain
- Determination of the common mode rejection ratio

EQUIPMENT REQUIRED

- base unit for the IPES system (power supply mod. PS1-PSU/EV, module holder structure for modules mod. MU/EV), individual control unit mod. SIS1/SIS2/SIS3
- experiment module mod. MCM5/ EV
- function generator
- oscilloscope
- multimeter.

B28.1 BASIC THEORY

A differential amplifier consists basically of two transistors with emitters connected to a single resistance (figure B28.1).

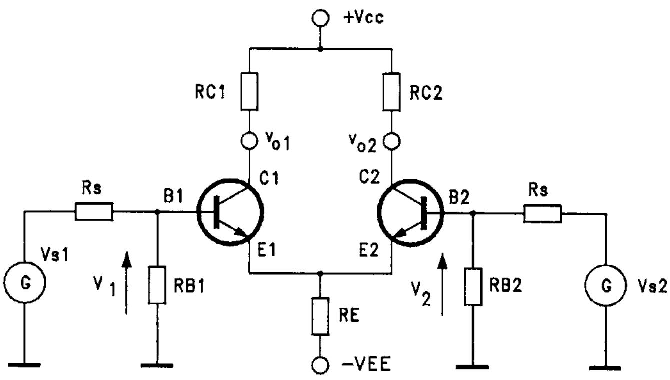


fig.B28.1

The differential amplifier amplifies the voltage difference between the inputs of the two transistors. Usually it has two input signals but only one output. The output can be taken from two different points:

- between the collector of a transistor and the ground of the circuit. This output is called "common mode ":

$$V_o = V_{o2}$$

- between the two collectors. The output is called then "floating" as it is not referred to ground:

$$V_o = V_{o1} - V_{o2}$$

Operation

A differential amplifier is generally symmetrical in its connections as well as in the values of the components. In the circuit of figure B28.1, we have $R_{C1}=R_{C2}$, $R_{B1}=R_{B2}$, T1=T2. With this symmetry we can say that voltage gains of the 2 amplifiers considered separately, are equal. So:

$$v_o = A_1 \cdot v_1 - A_2 \cdot v_2 = A_d \cdot (v_1 - v_2)$$

where A_d is called *differential mode gain.*

In practice the two signals v_1 and v_2 are not amplified by exactly the same amount ($A_1 \neq A_2$). This means that even if the two input signals are equal, the output will be different from zero.

To evaluate the differential amplifier we could use the previous formula with different values A_1 and A_2. However it is generally preferred to note that, if $A_1 \neq A_2$, then not only the difference between the two signals, but also their half sum, is amplified, i.e.:

$$v_o = A_d \cdot (v_1 - v_2) + A_c \cdot \frac{v_1 + v_2}{2} = A_d \cdot v_d + A_c \cdot v_c$$

using the following definitions :

$A_d = (A_1 + A_2)/2$	differential mode gain
$A_c = A_1 - A_2$	common mode gain
$v_d = v_1 - v_2$	differential mode signal
$v_c = (v_1 + v_2) / 2$	common mode signal

Common Mode Rejection Ratio - CMRR

The closer A_1 is to A_2, the better the differential amplifier is, (alternatively the greater A_d is compared to A_c). The quality of the amplifier is then expressed by the ratio between A_d and A_c, called the *Common Mode Rejection Ratio* (CMRR):

$$CMRR = | Ad/Ac |$$

The greater CMRR, the more the output signal will be proportional to the difference between the two input signals.

B28.2 EXERCISES

➲ *MCM5*	**Disconnect all jumpers** **Set in OFF all S switches**
➲ *SIS1*	**Turn all switches *OFF***
➲ *SIS2*	**Insert lesson code: B28**

Biasing

- Set Vcc adjustable power supply to 12V.
- Insert jumpers J4, J15, J18, J23, J26, J38, J34, J45, J43 to produce the circuit of fig.B28.2
- set RV4 to mid-position

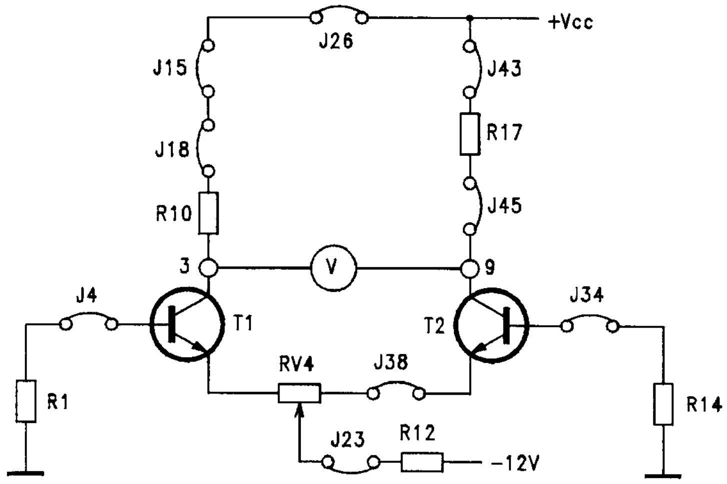


fig.B28.2

- measure the voltage between the collectors of the 2 transistors

  A zero voltage should be measured, but due to inevitable asymmetries of the circuit it is almost certain that the voltage read is different from zero

- adjusting trimmer RV4, set the voltage read by the voltmeter to zero

  The trimmer RV4 enables the current through the two transistors to be equalised, and so sets the voltage between the collectors to zero.

Differential gain

- Insert also jumpers J27 and J30, to produce the circuit of figure B28.3.
- adjust RV5 trimmer to measure 0 V between base and ground of T2
- adjusting RV4 trimmer, carefully balance the differential amplifier (voltage measured between the two collectors equal to zero)
- adjusting RV5, increase the input voltage on transistor T2 to reach 100 mV
- in these conditions, measure the corresponding voltage value between the two collectors, and calculate the voltage gain
- repeat the last measurement and calculation for increasing input voltage values :(150, 200, 400 mV)

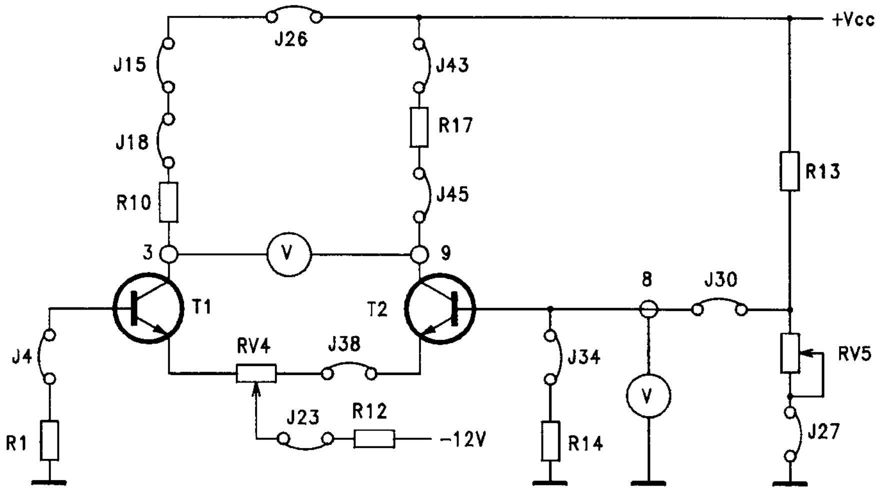


fig. B28.3

Q1 *What is the gain you have just measured?*

SET

A	*B*	
1	5	it is zero
2	4	it is unity
3	1	it is some tens
4	2	it is some hundreds
5	3	it is some thousands

Common mode gain

- From previous circuit, insert jumper J32, to obtain the circuit of fig.B28.4
- adjusting RV5 set the input voltage of the two transistors T1 and T2 to 0 V
- adjusting RV4 trimmer, balance the differential amplifier (null voltage between the two collectors T1 and T2)
- adjusting RV5, progressively increase the input voltage on the two transistor T1 and T2, and measure the output voltage between the two collectors
- calculate the common mode gain A_c

Q2 *Comparing the gains found in the last two exercises, we see that:*

SET

A	*B*	
1	4	the two gains are perfectly equal
2	1	the gain obtained from the second measurement is much higher than in the first case
3	2	the gain obtained in the second case is much smaller than the first case
4	5	the gain of the second measurement is zero, the one in the first is infinite
5	3	none of the above describes the result

CMRR

- With the gain values found from the last points, calculate the common mode rejection ratio in the differential amplifier under test

The common mode rejection ratio CMRR, is a parameter indicating the quality of a differential amplifier. As it is defined by the ratio CMRR = A_d / A_c, for an ideal amplifier it is infinite.

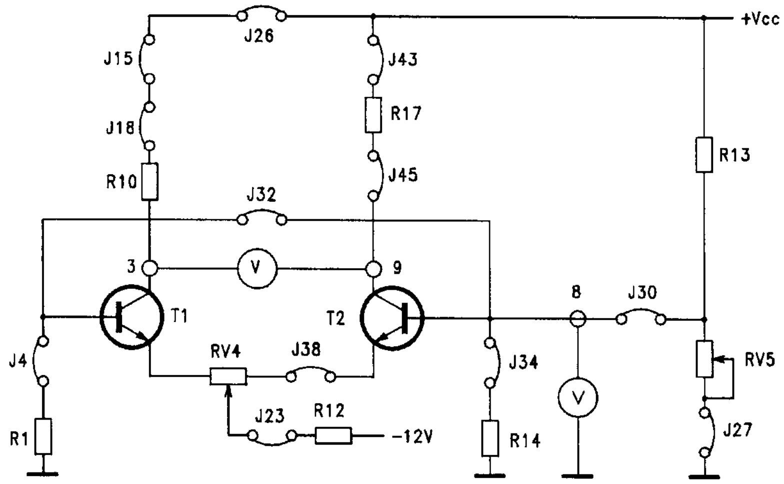


fig. B28.4

Small signal amplifier

- Remove jumpers 27, J30, J32, insert J1, J2 to produce the circuit of figure B28.5.

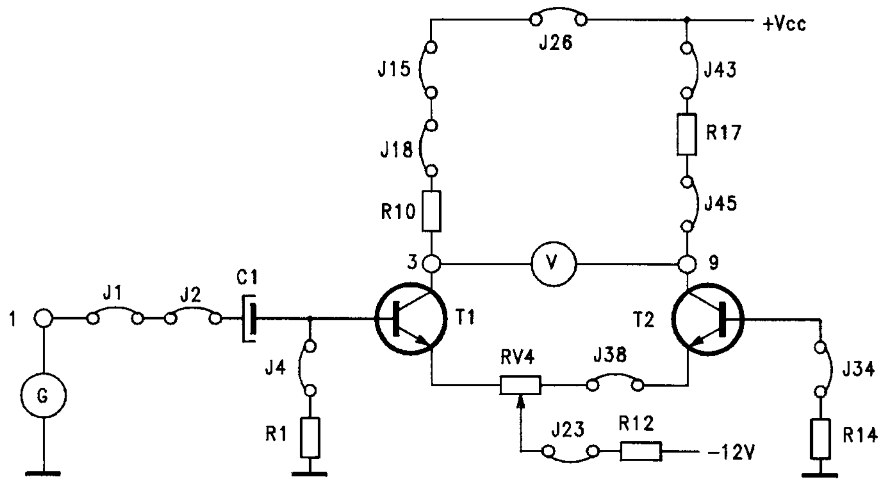


fig. B28.5

- adjust the RV4 trimmer to balance the circuit (null voltage between the collectors of the two transistors)
- Connect the function generator at terminal 1 and ground with a sine wave, 1 KHz and 400mVpp.
- Connect the oscilloscope channel 1 at terminal 1 (input signal) and channel 2 at terminal 3 (output signal on T1 collector).
- measure the collector voltage amplitude, and the phase difference between this voltage and the input signal
- repeat the last measurement for the transistor T2, connect channel 2 at terminal 9 (output signal on T2 collector).

Q3 *What is the relation between the two voltages measured on the collectors?*

SET

A	*B*	
1	2	they are equal in amplitude and phase
2	1	they are equal in amplitude, but are 180 degrees apart
3	5	they are in phase but one is twice the other
4	3	they are shifted by 90 degrees and one is half the amplitude of the other
5	4	they are equal in amplitude and shifted by 270 degrees

Q4 *What is the ratio of the signal taken between the 2 collectors, to that of the signal taken between a collector and ground ?*

SET

A	*B*	
1	5	the amplitude of the signal between the two collectors is half the one measured between each collector and ground
2	3	the amplitude between the collectors is double the one between a collector and ground
3	1	the three amplitudes are exactly the same
4	2	the amplitudes are equal, but each is shifted by 120 degrees compared to another
5	4	the three amplitudes are all quite different

Temperature stability

- In the previous circuit, disconnect the function generator and the oscilloscope, to take the circuit back to the configuration in figure B28.2
- adjusting trimmer RV4, balance the circuit
- with the help of a thermal source, lightly heat T1, and simultaneously note the voltage variation taken between the collectors (connect the positive terminal of the voltmeter to the collector of T1)
- wait until the transistor T1 is cooled and repeat the test on the transistor T2
- you should note that the heating of T1 causes a drop in the measured voltage, but with T2 an increase occurs

The temperature increase of a transistor means an increase in its conduction, and so an unbalancing of the differential amplifier. If the two active devices which constitute the amplifier are thermally coupled, the circuit is insensitive to thermal variation. This coupling is achieved with integrated circuits.

B28.3 SUMMARY QUESTIONS

Q5 *An ideal differential amplifier amplifies:*

SET

A	*B*	
1	1	the difference between the two input voltages
2	5	the sum of the two input voltages
3	4	the product of the two input voltages
4	2	the half-sum of the input voltages
5	3	the ratio between the input voltages

Q6 *Starting from the input voltages v_1 and v_2 of a differential amplifier, how is the "common mode signal" defined?*

SET

A	*B*	
1	2	$v_c = (v_1 + v_2)/2$
2	1	$v_c = v_1 - v_2$
3	5	$v_c = v_1 + v_2$
4	3	$v_c = v_1 \cdot v_2$
5	4	$v_c = (v_1 \cdot v_2)/2$

Q7 *And how is the differential mode signal defined?*

SET

A	*B*	
1	2	$v_d = (v_1 + v_2)/2$
2	1	$v_d = v_1 - v_2$
3	4	$v_d = v_1 + v_2$
4	5	$v_d = v_1 \cdot v_2$
5	3	$v_d = v_1 \cdot v_2 / 2$

Q8 *Which relation defines the output of a differential amplifier, if v_1 and v_2 are the voltages across the two inputs?*

SET

A	*B*	
1	5	$v_o = A_d \cdot v_d - A_c \cdot v_c$
2	4	$v_o = (A_d \cdot v_d + A_c \cdot v_c)/2$
3	3	$v_o = A_d \cdot v_d + A_c \cdot v_c$
4	2	$v_o = (A_d/2) \cdot v_d + 2 \cdot A_c \cdot v_c$
5	1	$v_o = (A_d + A_c) \cdot (v_d - v_c)$

Lesson B29: CLASS A AMPLIFIERS

OBJECTIVES

- To understand power and efficiency in the static (dc) and dynamic (ac) case
- to observe distortions due to transistor saturation and cut-off

EQUIPMENT REQUIRED

- base unit for the IPES system (power supply mod. PS1-PSU/EV, module holder structure for modules mod. MU/EV), individual control unit mod. SIS1/SIS2/SIS3
- experiment module mod. MCM5/ EV
- function generator
- oscilloscope
- multimeter.

B29.1 BASIC THEORY

In a class A amplifier, the operating point and the input signal are such that current flow in the output circuit is always present. This kind of amplifier operates essentially in the linear zone. If base current variations, caused by the input signal, are small enough to keep within the linear region, the output wave-form faithfully reproduces the input .

The collector current flows for the entire duration of the of the input signal, and its average value is identical to the quiescent one.

Figure B29.1 shows the typical curves of an amplifier with transistor in class A: the output characteristic of the transistor; load line; input signal (base current i_b); output signal (collector-emitter voltage v_{ce}).

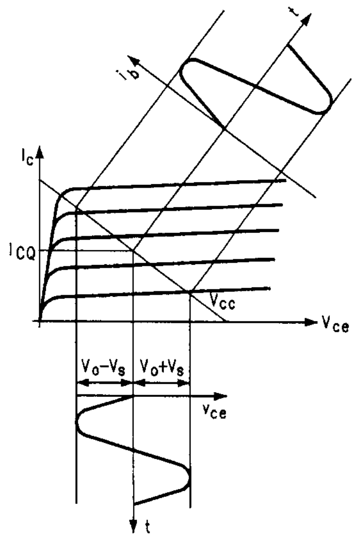


fig.B29.1

Power

To find the powers used in a class A amplifier, suppose that the amplifier circuit of figure B29.2 has a quiescent voltage V_{CEQ} equal to Vcc/2, and the corresponding current is $I_{CQ} = Vcc \cdot R_L/2$.

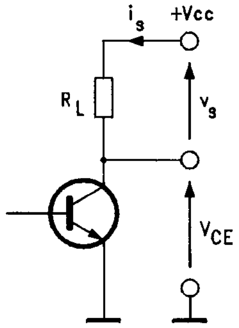


fig.B29.2

1. *Useful power Pu*

considering sine signals, the variable voltage on load R_L is $V_S \cdot \sin(w \cdot t)$ and the total voltage is :

$v_s(t) = V_0 + V_S \cdot \sin(\omega \cdot t)$

The power dissipated on the load R_L is equal to the average value of the instantaneous power $v_s(t) \cdot i_s(t)$:

$$P_{RL} = \frac{Vcc^2}{4 \cdot R_L} + \frac{V_S^2}{2 \cdot R_L}$$

Considering only the power related to the signal, we have :

$Pu = V_S^2 / (2 \cdot R_L)$

2. *Power Pcc supplied by the power supply*

This is the average power value ($Vcc \cdot i_s$) provided by the power supply, and is equal to:

$Pcc = Vcc^2/(2 \cdot R_L)$

3. *Power dissipated by the transistor P_D*

This is the average value of the power dissipated in the transistor [$v_{ce}(t) \cdot i_s(t)$]:

$$P_D = \frac{Vcc^2}{4 \cdot R_L} - \frac{V_S^2}{2 \cdot R_L}$$

As you can note, P_D is a minimum if the a.c. signal amplitude is maximum.

Efficiency

This is defined as the ratio between the useful power in the load (Pu) and the power supplied by the power supply (Pcc):

$\eta_c = Pu/Pcc = V_S^2/Vcc^2$

From this we can say that the efficiency is max. when V_S is max. In theory, V_{Smax} is equal to (Vcc/2); in this ideal condition the efficiency is 25%. In practice, the efficiency of class A amplifiers is limited to about 20%.

Higher efficiencies from a class A amplifier (max 50%) are obtained if the load is coupled using a transformer, as examined in lesson B24.

B29.2 EXERCISES

➲ *MCM5*	**Disconnect all jumpers** **Set in OFF all S switches**
➲ *SIS1*	**Turn all switches *OFF***
➲ *SIS2*	**Insert lesson code: B29**

- Set Vcc adjustable power supply to 20V.
- Insert jumpers J1, J2, J5, J6, J11, J17, J26, and the multimeter (function IDC) between terminals 4 and 5 to produce the circuit of figure B29.3

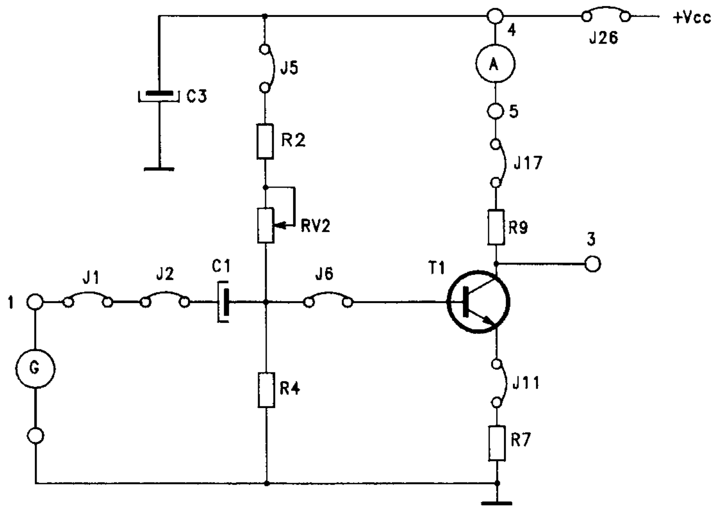


fig.B29.3

- adjust RV2 to obtain $I_{CQ} = 9$ mA
- connect the oscilloscope channel 1 at terminal 1 (input signal of the amplifier) and channel 2 at terminal 3 (output signal).
- Connect the function generator at terminals 1 and ground with a sine wave, 1 KHz and 1.5Vpp.
- check that with this amplitude, the output value does not have large distortions (it should be as in figure B29.4a)
- increase the input signal and check the behavior of the output signal

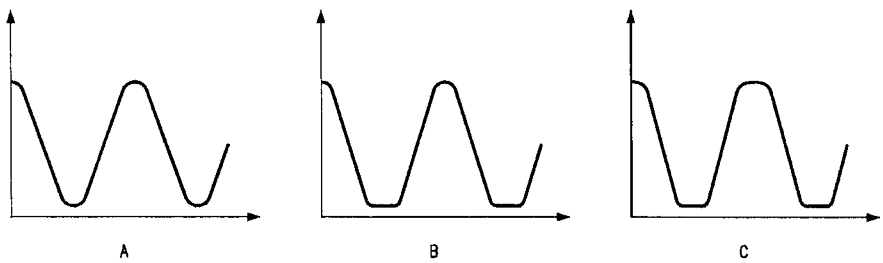


fig.B29.4

Q1 *What happens to the output signal, and what is the reason for this?*

SET		
A	*B*	
1	3	the signal is unchanged
2	5	the signal has distortions on the negative half-waves due to the fact that the transistor reaches the cut-off zone
3	4	distortions are noticed on the positive half-waves when the transistor is cut-off
4	1	spurious pulses of short duration and high amplitude occur due to high frequency disturbances
5	2	distortions are noticed on both half-waves due to the large excursions of the input signal which takes the transistor into either saturation or cut-off state

The distortions illustrated in fig.B29.4b/c, are due to the non-linearity of the transistor, when its operation is close to, or reaches, the cut-off or saturation zones.

- Adjust the input voltage to obtain a signal with max. amplitude at the output, but which has no significant distortion
- measure the V_S signal amplitude = $V_{S}pp/2$
- with this value, calculate :
  - the useful power on the load $Pu = V_S^2/2 \cdot R_L$
  - the power dissipated in the transistor P_D
  - the power supplied by the power supply Pcc
  - the efficiency "η" of the circuit

Q2 *What is the efficiency η, approximately?*

SET		
A	B	
1	6	about 0.5%
2	1	about 1%
3	4	about 7.5%
4	3	about 20%
5	2	about 45%
6	5	about 75%

- vary the biasing and note the variation in the output wave-form.

B29.3 SUMMARY QUESTIONS

Q3 *Consider an amplifier in class A, with a sine wave input. The collector current flows for a time equal to:*

SET

A	*B*	
1	3	half of the cycle
2	6	1/4 cycle
3	4	3/4 cycle
4	5	2.5 cycles
5	2	none of the cycle
6	1	the entire cycle

Q4 *A signal amplified in class A may have distortions due to:*

SET

A	*B*	
1	6	transistor saturation and cut-off
2	5	frequency operation limitation of the transistor
3	2	presence of parasitic capacitances of the transistor
4	1	too low efficiency
5	4	too low temperature
6	3	none of the above

Q5 *If Vcc is the power supply voltage of an amplifier in class A, and if V_0 is the quiescent voltage across the load, the output signal of amplitude V_S is distorted if:*

SET

A	*B*	
1	1	$V_S > (Vcc - V_0)$
2	5	$V_S < V_0$
3	2	$(Vcc + V_0)/4 > V_S$
4	3	$V_S < (Vcc - V_0)$
5	4	$V_S < V_0/2$

Q6 *The efficiency of a class A amplifier, with load not coupled through a transformer:*

SET

A	*B*	
1	2	depends on the phase angle
2	1	can take the max. theoretical value of 25 %
3	4	is always equal to 1
4	5	can take a theoretical value equal to 50 %
5	3	depends on the load and the signal frequency

Lesson B30: CLASS B AMPLIFIERS

OBJECTIVES

- Study of a "single-ended" circuit
- Study of a "Push-pull" circuit

EQUIPMENT REQUIRED

- base unit for the IPES system (power supply mod. PS1-PSU/EV, module holder structure for modules mod. MU/EV), individual control unit mod. SIS1/SIS2/SIS3
- experiment module mod. MCM5/ EV
- function generator
- oscilloscope
- multimeter.

B30.1 BASIC THEORY

The low efficiency of amplifiers in class A arises from the fact that, even in absence of a signal, the transistor dissipates power. The solution to this problem is obtained by fixing the Q point close to the cut-off state. In this case when the input signal is missing, the collector current will be very low. However when the signal is present a current flows corresponding to the positive half cycle of the applied signal. Each negative excursion of the input signal, being less than the cut-off value, cause a total block of the collector current. Figure B30.1 shows an example of amplification of an a.c. signal in class B.

In case of a.c. signal, the collector current flows for only about half a cycle, i.e. 180 degrees. This angle constitutes the so called *conduction angle.* For an output signal is to be obtained similar to the input one, two active devices must be used biased in class B. Each of them must amplifies one half of the wave. There are three types of circuit based on this principle :

- push-pull
- single-ended
- complementary symmetry.

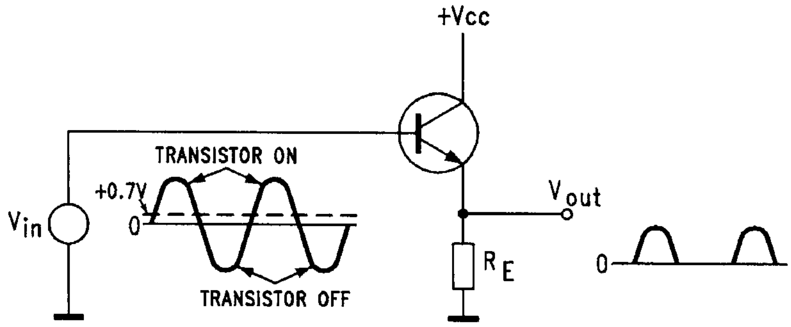


fig.B30.1

Single-Ended Amplifier with dual power supply

The single-ended connection is show in figure B30.2

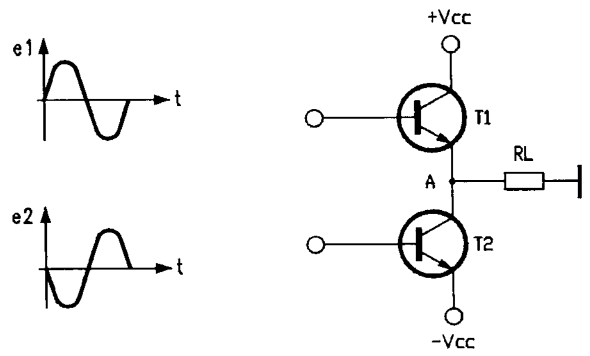


fig.B30.2

In the quiescent state, the two transistors are cut-off and their common point A is ground. No current flows in the load.
In dynamic operation, T1 conducts on the positive half-cycle and current flows from left to right through the load. In the negative half-cycle T2 will conduct, causing a current to flow through the load in the opposite direction. For this to happen, and faithfully reproduce the signal, it is necessary to supply the bases of the two transistors with two signals in phase opposition.

When determining component values, remind that across the cut-off transistor the voltage is twice Vcc (since the voltage drop V_{CE} is almost zero across the transistor in conduction). The transistors must be chosen with $BV_{CEO} > 2 \cdot Vcc$ (BV_{CEO} = breakdown voltage).

As for the input signals, the two transistors cannot be controlled by two signals referred to ground, because in this case T1 would operate as follower and T2 as common emitter, and the two half-waves on the load would have different amplitudes.

To make T1 operate as common emitter, it is necessary to apply the signal between base and emitter. This can be done with the transformer coupling of figure B30.3.

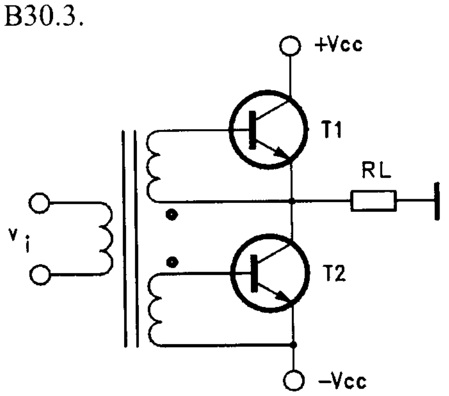


fig.B30.3

Single-Ended Amplifier with single power supply

To use a single power supply voltage (figure B30.4), the load must be connected to a very high capacitance (some hundreds of μF). In this way the voltage across the capacitance stays constant during dynamic operation, simulating the behavior of a second power supply.

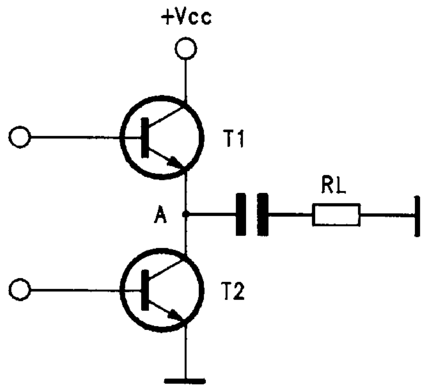


fig.B30.4

If the transistors are identical, then at the Q point the common connection A is at a voltage of Vcc/2, and the capacitor is kept charged to that voltage.

The operation is the same as one with two power supplies. When T1 conducts, the power supply voltage for the circuit is the difference between Vcc and Vcc/2 supplied by the capacitor, i.e. in total Vcc/2. When T2 is conducting, the only power supply operating is the one supplied by C, i.e. it is still Vcc/2.

Push-Pull Amplifers

The Push-Pull circuit consists of two NPN transistors which are symmetrically connected and have a common emitter (figure B30.5). Across the output of the two stages there is a signal transformer with a central tapping. As the transistors are of the same kind, each collector current flows only in its half of the transformer, i.e. they are in in opposite directions and so produce two opposed flows.

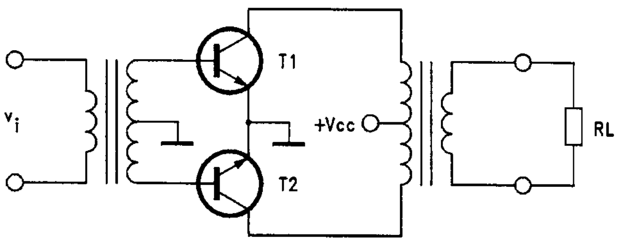


fig.B30.5

In static operation, as the two transistors operate in class B, they are both Off.

Now consider the ac or dynamic operation, and suppose that each transistor alternatively conducts for each half-wave. As the two half-waves in the transformer secondary are in opposition, the complete sine-wave is reconstructed in the load.

A system must be used which makes the two BJTs conduct alternatively. An input transformer with central tapping is often used, which provides the transistor bases with two equal signals, of opposite phase. One alternative to the input transformer is to use an electronic type of phase inverter as used in the dual-load amplifiers. This will have a better frequency response than a transformer.

Power calculations

1. *Useful power Pu*

   When the voltage across the load R_L has max. amplitude V_M, the useful power dissipated in the load is :

   $Pu = V_M^2 / 2 \cdot R_L$

2. *Power Pcc supplied by the power supply*

   This is the average value of the power supplied by the power supplies, and is:

   $Pcc = 2 \cdot Vcc \cdot V_M / (\pi \cdot R_L)$

   From this you can see that Pcc is max. when V_M is max., i.e. equal to Vcc. So

   $Pcc = 2 \cdot Vcc^2 / (\pi \cdot R_L)$

3. *Power dissipated in the transistor P_D*

   This is the average value of the power dissipated in each transistor:

   $$P_D = \frac{Vcc \cdot V_M}{\pi \cdot R_L} - \frac{V_M^2}{4 \cdot R_L}$$

   P_D is max. if $V_M = 2 \cdot Vcc/\pi$. So :

   $P_{Dmax} = Vcc^2 / \pi^2 \cdot R_L$

   which corresponds approximately to $P_{umax}/5$.

4. *Efficiency*

It is defined as the ratio between the useful power on the load Pu and that supplied by the power supply Pcc:

$\eta = Pu / Pcc = \pi \cdot V_M / (4 \cdot Vcc)$

From this we see that the efficiency is a linear function of V_M, and is max. for V_M = Vcc ($\eta_{max} = \pi/4 = 78.5\%$). The practical efficiency of the amplifiers in class B is actually around the 70% mark.

Cross-over distortion

The base-emitter junctions prevent the transistors from amplifying signals with an amplitude less than the threshold voltage. Figure B30.6 shows the transfer characteristic of an amplifier with two BJTs.

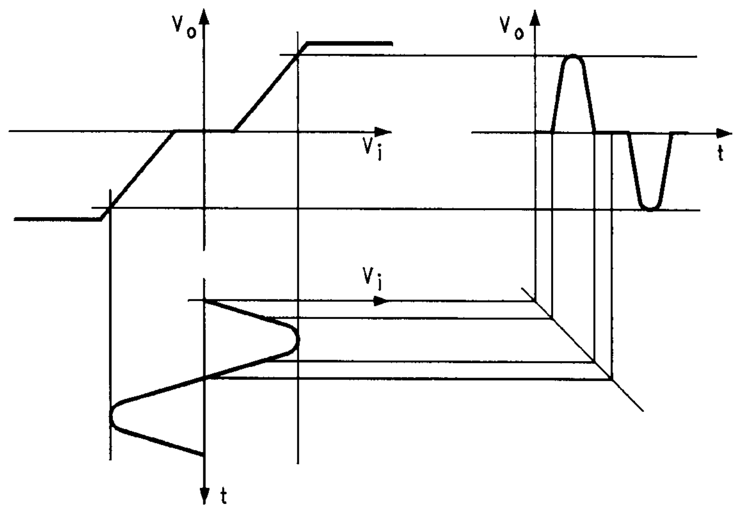


fig.B30.6

As can be seen from the output characteristic, the signal suffers distortion when passing through zero. This type of distortion is known as *cross-over distortion.* To overcome this, the BJTs are biased just to the threshold voltage. This type of biasing is called "class AB".

B30.2 EXERCISES

➲ *MCM5*	**Disconnect all jumpers** **Set in OFF all S switches**
➲ *SIS1*	**Turn all switches *OFF***
➲ *SIS2*	**Insert lesson code: B30**

Single-ended amplifier with a single power supply

- Insert jumpers J54, J55, J56, J57 to obtain the circuit of figure B30.7

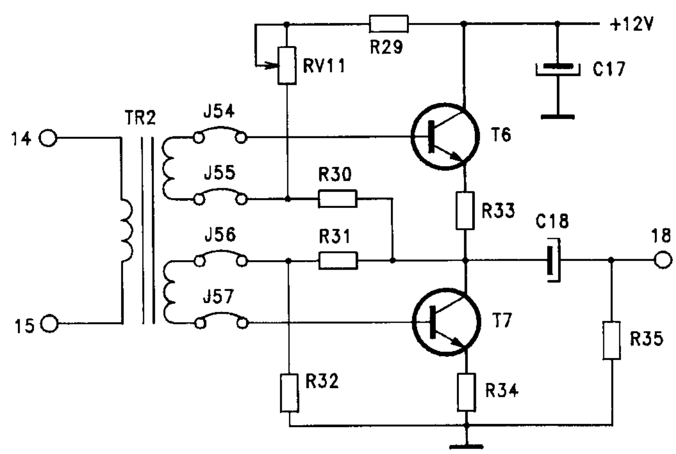


fig. B30.7

- adjusting trimmer RV11, take the collector voltage of the transistor T7 to 6 V

Q1 *In this condition, what is the current through the load R35 ?*

SET

A	*B*	
1	3	the current is 10 mA
2	5	the current is 100 mA
3	1	the current is zero
4	2	the current is 1 A
5	4	none of the above

- measure the voltage across R33 and R34: it should be very low, indicating almost zero current. The two transistors are biased to the cut-off region
- connect the function generator at terminals 14 and 15 with a sine wave, 1 KHz and 4 Vpp.
- measure the amplitude of the output signal; check if the output is distorted, and calculate the gain of the amplifier

➲ *SIS1*	**Turn switch SW6 *ON***
➲ *SIS2*	**Press *INS***

Q2 *What is the effect on the output signal?*

SET		
A	*B*	
1	6	the signal goes to zero
2	1	the signal becomes continuous
3	4	the cross-over distortion increases
4	5	the negative half-waves of the output signal are eliminated
5	3	the signal has distortions on the positive half-waves
6	2	none of the above describes the results

Q3 *What is the reason for this?*

SET		
A	*B*	
1	5	the power supply has been disconnected from the circuit
2	3	collector and emitter of the transistor T6 are in short circuit
3	4	the biasing of transistor T7 has been removed
4	2	100 Ω resistance has been set in parallel to the resistance R30
5	1	the output capacitor C18 has been short-circuited

➲ *SIS1*	**Turn switch SW6 *OFF***

Power calculations

- Adjust the function generator to obtain a signal with max. amplitude, but without distortions
- using the formulas supplied in the theoretical section, calculate the values of :
  - Useful power Pu
  - Power Pcc supplied by the power supply
  - Power dissipated in the transistor PD

Push-pull Amplifiers

Biasing

- Switch off PS1-PSU power suply and remove all jumpers.
- Insert J48, J49, J50, J51, J52, J53, to obtain the circuit of figure B30.8
- before connecting power, adjust the trimmers RV9 and RV10 to mid-position
- switch on the power and adjust trimmer RV8 to obtain a voltage V_{CEQ} of about 5 V across T3
- adjust RV9 so that the d.c. voltages present across the bases of the two transistors T4 and T5 are equal

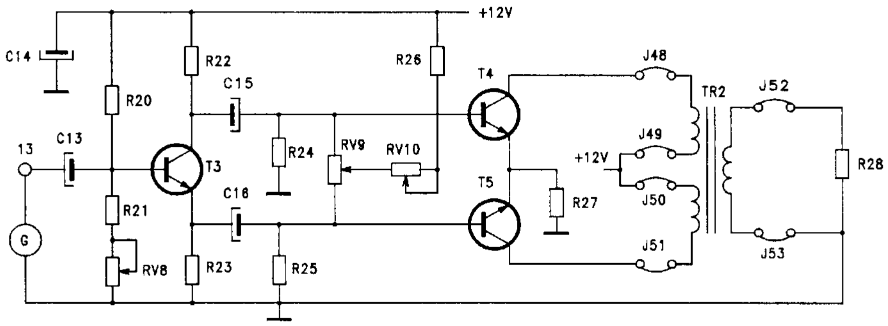


fig. B30.8

- connect the function generator at terminals 13 and ground with a sine wave, 1 KHz and 4 Vpp
- connect the oscilloscope channel 1 at terminal 13 (input signal) and channel 2 across R28 (output signal)
- adjust RV10 to obtain the max. amplitude of the output signal, but with minimum distortion

Q4 *What differences can be noticed between the two signals?*

SET

A	*B*	
1	2	they are equal in amplitude, but phase shifted by 180°
2	1	they are in phase, but the output amplitude is half the input one
3	3	the output signal is higher than the input one, but has small distortions when passing through zero
4	5	they are equal in amplitude, but the output one has double frequency of the input
5	4	the input signal has double the amplitude of the output, and has distortions on the positive half-waves.

Adjusting RV10, it is possible to reduce the distortion occurring around zero (cross-over distortion), while RV9 can be used to vary the symmetry.

The output transformer produces an output signal in phase with, or in opposition to the input, depending on which way the transformer is connected.

➲ *SIS1*	**Turn switch SW10 *ON***
➲ *SIS2*	**Press *INS***

Q5 *By considering the change in the signals displayed on the oscilloscope, we can say that:*

SET

A	*B*	
1	2	the power supply voltage is reduced by half
2	5	the input signal has been removed
3	4	the base and emitter of T3 are short-circuited
4	1	the emitter resistance of T3 has changed
5	3	the collector and emitter of T4 are short-circuited

➲ *SIS1*	**Turn switch SW10 *OFF***

- display the output signal across R28, and the collector voltage of T3 on the oscilloscope
- increase the amplitude of the input signal to observe distortions on the output signal, distortions which are caused by the transistor operating in the saturation region
- check that these distortions are due to the saturation of the first inverter stage, and not to the final transistors

➲ *SIS1*	**Turn switch SW4 *ON***
➲ *SIS2*	**Press *INS***

Q6 *The output signal has changed. What is the reason for this?*

SET

A	*B*	
1	2	the circuit has been disconnected at the collector of T4
2	3	the biasing of T4 and T5 is incorrect
3	4	the resistance R20 has been short-circuited
4	5	the static gain h_{FE} of transistor T5 has been changed
5	1	none of the above

➲ *SIS1*	**Turn switch SW4 *OFF***

Power calculations

- Display the output voltage across R28
- adjust the signal generator to produce a max output signal without distortion
- measure the amplitude V_M of the output signal, and calculate the useful power $Pu = V_M^2 / 2 \cdot R28$
- calculate the power supplied by power supply

$$Pcc = \frac{2}{\pi} \cdot \frac{Vcc}{R28} \cdot \frac{N2}{N1} \cdot V_M$$

where N1 = 220 turns; N2 = 700 turns (transformer data)

- calculate the power dissipated by one transistor: $P_D = (Pcc - Pu)/2$

B30.3 SUMMARY QUESTIONS

Q7 *The operation of an amplifier in class B is characterized by conduction angles:*

SET

A	*B*	
1	3	greater than 180 degrees
2	5	equal to 90 degrees
3	2	equal to 180 degrees
4	1	between 90 and 180 degrees
5	4	less than 180 degrees

Q8 *The operation of an amplifier in class A-B is characterized by conduction angles:*

SET

A	*B*	
1	2	greater than 180 degrees
2	1	equal to 180 degrees
3	4	less than 180 degrees
4	5	equal to 360 degrees
5	3	equal to 60 degrees

Q9 *To eliminate cross-over distortion in a Push-pull amplifier, you must:*

SET

A	*B*	
1	2	bias the bases of the transistors to the threshold voltage (class A-B)
2	1	slightly bias the circuit to class C
3	4	reduce the amplifier operating frequency
4	5	increase the amplitude of the input signal
5	3	double the power supply voltage

Lesson B31: PUSH-PULL, COMPLEMENTARY SYMMETRY AMPLIFIER

OBJECTIVES

- Study of a class B, push-pull, complementary symmetry amplifier
- resistive divider with dual-voltage power supply
- biasing of a diode divider in a single voltage supply circuit
- power calculations and voltage gain measurement

EQUIPMENT REQUIRED

- base unit for the IPES system (power supply mod. PS1-PSU/EV, module holder structure for modules mod. MU/EV), individual control unit mod. SIS1/SIS2/SIS3
- experiment module mod. MCM5/ EV
- function generator
- oscilloscope and multimeter.

B31.1 BASIC THEORY

The typical diagram of a class B, push-pull, complementary symmetry amplifier is shown in figure B31.1

It can be noted that the two transistors used are complementary (an NPN and a PNP), and both are connected as emitter follower. The load is driven by T1 during the positive half-cycles of the input signal, and by T2 during the negative ones (figures B31.2a and B31.2b).

fig.B31.1

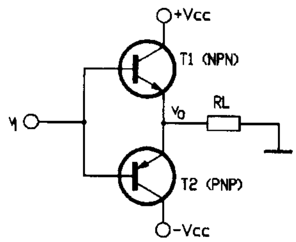


fig. B31.2a

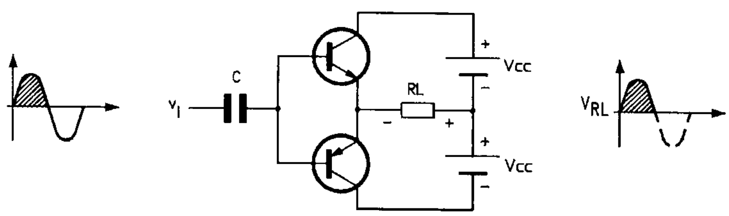
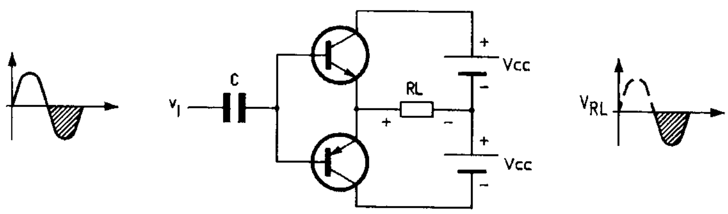


fig. B31.2b



Note that the input and output signals of the amplifier are in phase. There is also considerable cross-over distortion.in this kind of amplifier, like those seen in the last chapter,

The cross-over distortion is due to the fact that transistors T1 and T2 start conducting only when their voltage V_{BE} reaches the conduction threshold (0.7V). Conversely, they are cut-off when V_{BE} falls below 0.7V.

To limit cross-over distortion, a base bias circuit is required, in order to make the two transistors lightly conduct even in absence of signal. Figure B31.3 shows an example of a bias circuit to reduce cross-over distortion. The voltage V_{BE} on the two transistors is kept at 0.7V (threshold voltage) by the diodes D1-D2, which are hold in conduction by resistors R1-R2.

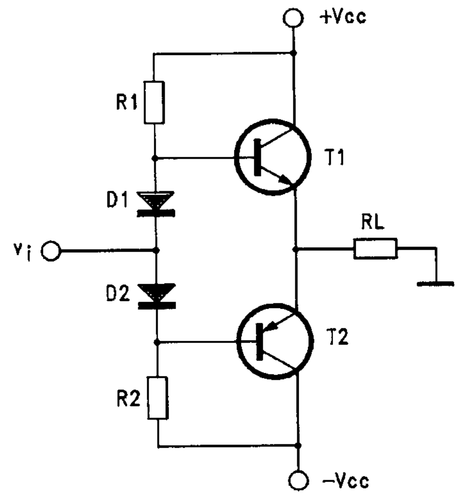


fig. B31.3

Using a single battery as power supply

Just like the "single-ended" circuit seen before, a single battery can be used for a complementary symmetry circuit, by connecting the load to a large capacitor (figure B31.4).

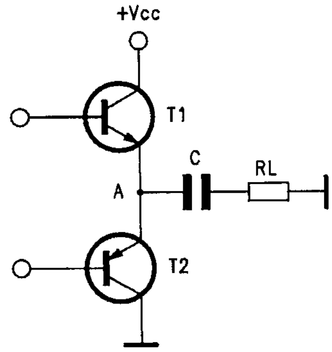


fig. B31.4

B31.2 EXERCISES

➲ *MCM5*	**Disconnect all jumpers** **Set in OFF all S switches**
➲ *SIS1*	**Turn all switches *OFF***
➲ *SIS2*	**Insert lesson code: B31**

Dual-voltage supply circuit

- Insert jumpers J58, J59, J61, J63, J70, J72, J73, J75, J76, and the multimeter (function IDC) between terminals 18 and 19, to produce the circuit of figure B31.5

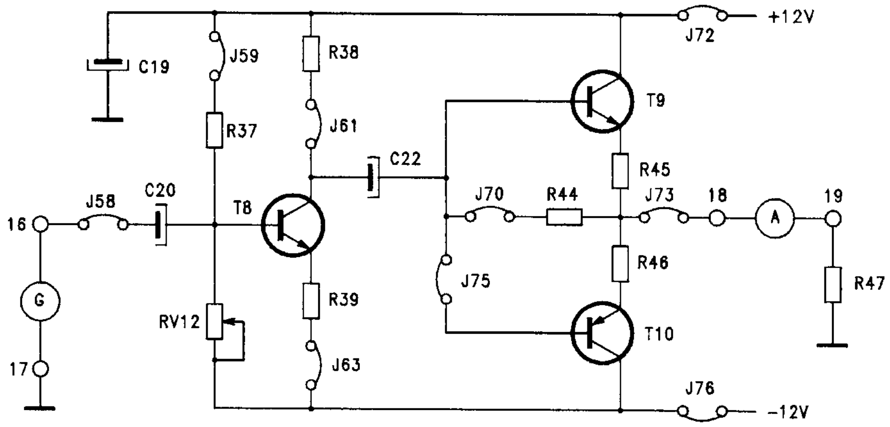


fig. B31.5

- before connecting the input signal to the circuit, measure the voltages V_{BE} and V_{CE} of both transistors, and the voltage across the output load (resistance R47)

Q1 *What is the operating state of the two transistors ?*

SET

A	*B*	
1	5	transistor T9 is cut off, transistor T10 is in saturation
2	1	transistor T9 is in active zone, T10 is in saturation
3	4	transistor T9 is in saturation, T10 is cut off
4	3	both transistors are cut off
5	2	both transistors are in the active region

- adjusting trimmer RV12, set the voltage V_{CEQ} of transistor T8 equal to 12 V
- connect the function generator at terminal 16 and ground point with a sine wave, 1 KHz and 1 Vpp (**!! Note: terminal 17 is not Ground in this circuit !!**)

- vary the amplitude of this input signal, and determine the saturation limits of the first stage T8
- reduce the voltage of the input signal so that the first stage is not saturating
- display the input and output signals of the amplifier on the oscilloscope

Q2 *What are the differences between the two signals?*

SET

A	*B*	
1	5	the two signals are equal in amplitude and phase
2	1	the input signal has a higher amplitude than the output
3	4	the output signal is three times the frequency of the input
4	2	the output signal has a higher amplitude than the input, but has cross-over distortion
5	3	the output signal goes to zero in the positive half-cycles of the input signal

- From previous circuit, remove jumpers J70, J75 and insert J65, J67, J69, so to produce the diagram of figure B31.6

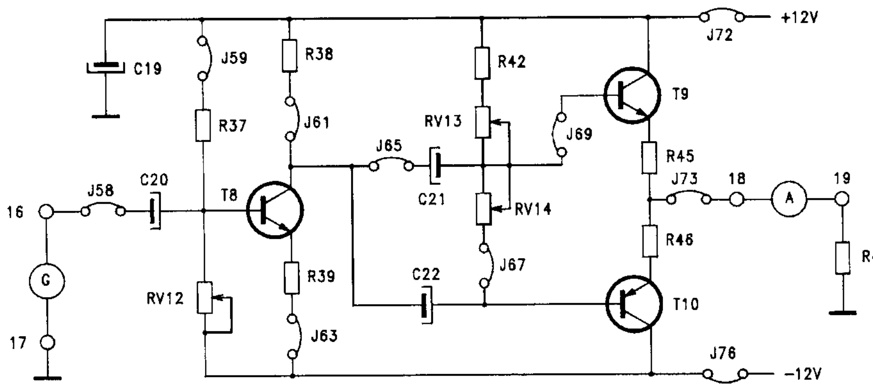


fig. B31.6

- adjust RV12 to obtain a voltage V_{CEQ} for transistor T8 of about 12 V
- adjust RV13 and RV14 to mid-position
- display the d.c. voltage across load R47 on the oscilloscope, and observe the changes caused by adjusting trimmer RV13

Trimmer RV13 controls the transistor biasing, and allows to set the d.c. output component in R47 to zero.

- Apply a sine wave input signal with 2Vpp-amplitude and 1KHz-frequency
- check that adjustment of trimmers RV13 and RV14 produces changes in the output signal

➲ *SIS1*	**Turn switch SW8 *ON***
➲ *SIS2*	**Press *INS***

Q3 *Considering the change to the output signal, what is the possible cause?*

SET

A	*B*	
1	3	the collector and emitter of T8 are short-circuited
2	5	the base and emitter of T9 are short-circuited
3	1	the collector and emitter of T9 are short-circuited
4	2	C20 has been disconnected
5	4	the negative half-cycles on the load have a lower amplitude, since the value of R46 has increased

➲ *SIS1*	**Turn switch SW8 *OFF***

Single voltage supply: using diodes to remove cross-over distortion

- Set Vcc adjustable power supply to 24V.
- Remove all jumpers, insert J60, J62, J64, J66, J68, J71, J74, J77, to produce the circuit of figure B31.7

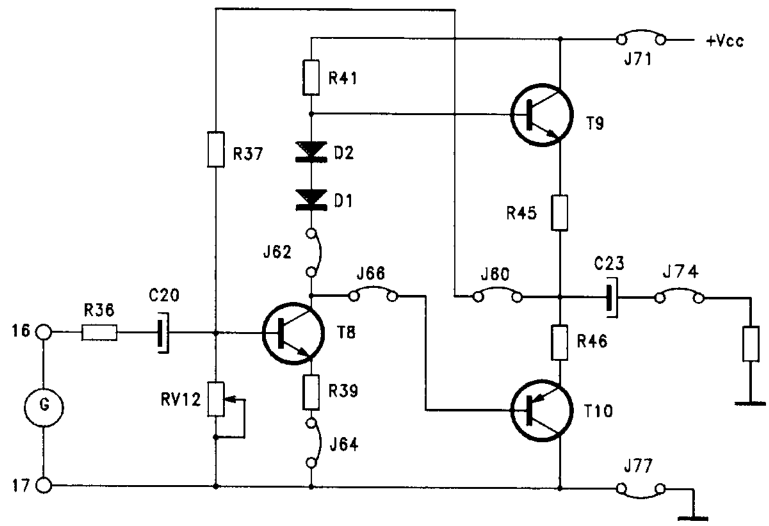


fig. B31.7

- adjust RV12 to obtain a d.c. voltage of 10V at the transistor collector T8
- check that the voltage between the common point of the two resistors R45 and R46 and ground is about 10.7 V, i.e. the collector voltage of transistor T8 plus the bias voltage V_{BE} of transistor T10

- measure the voltage V_{CEQ} of the transistors T9 and T10, and the voltages across their emitter resistances, in order to calculate the current flowing.

Q4 *From this data the operating state of transistors T9 and T10 can be found :*

SET		
A	*B*	
1	4	T9 is cut-off, T10 is in saturation
2	3	T9 is saturated, T10 is cut-off
3	1	both transistors are cut off
4	2	both transistors are in saturation
5	5	both transistors are in the active zone

- connct the function generator at terminals 16 and 17 with a sine wave, 1 KHz and 4Vpp
- check if the output is free from cross-over distortion

➲ ***SIS1***	**Turn switch SW11 *ON***
➲ ***SIS2***	**Press *INS***

Q5 *What is the reason for the amplifier malfunction ?*

SET		
A	*B*	
1	5	the diode D1 is disconnected
2	3	the transistor T9 is disconnected
3	4	RV12 is short-circuited to ground
4	2	base and emitter of T8 are short-circuited
5	1	the power supply is missing in the circuit

➲ ***SIS1***	**Turn switch SW11 *OFF***

B31.3 SUMMARY QUESTIONS

Q6 *The complementary symmetry differs from the Push-pull and Single-ended circuit in that :*

SET

A	*B*	
1	5	phase inverter circuit is not required
2	3	a phase inverter circuit is required
3	1	it can be used with one or two batteries
4	2	it provides much higher efficiencies
5	4	it has a wider frequency response

Q7 *To produce a class B amplifier with a single voltage supply source, the one essential element is :*

SET

A	*B*	
1	3	a much smaller battery
2	5	a capacitor on the power supply
3	2	a capacitor in series with the output
4	1	no circuit modification is necessary
5	4	a diode in series with the bases of the transistor

Q8 *How do the two final transistors operate, in a complementary symmetry circuit?*

SET

A	*B*	
1	6	they simultaneously conduct on the positive half-cycle
2	5	they simultaneously conduct in the negative half-cycle
3	1	they alternately conduct for one cycle
4	3	they only conduct if the input signal is added to a positive signal
5	4	they conduct if the power supply voltage is lower than $2 \cdot V_{CEO}$
6	2	they conduct alternately, for one half cycle

Lesson B32: CLASS C AMPLIFIERS

OBJECTIVES

- Amplification with resistive loads:
  - analysis of the bias circuits
  - inspection of the current wave-form in the load
  - measurement of the conduction angles as a function of the biasing
- Amplification with tuned loads:
  - calculation of the resonant frequency fo
  - use as frequency multiplier

EQUIPMENT REQUIRED

- base unit for the IPES system (power supply mod. PS1-PSU/EV, module holder structure for modules mod. MU/EV), individual control unit mod. SIS1/SIS2/SIS3
- experiment module mod. MCM5/ EV
- function generator
- oscilloscope
- multimeter.

B32.1 BASIC THEORY

In class C amplifiers the transistor is biased in the cut-off region. With a sine signal as input, the output will consist of pulses with duration less than half a cycle (figure B32.1). The distortion introduced by this situation is very high. The operation of an amplifier in class C is decidedly non-linear.

Amplifiers in class C are mostly used with a resonant load, and around the resonant frequency of this load. Their use is limited to high frequency power amplification.

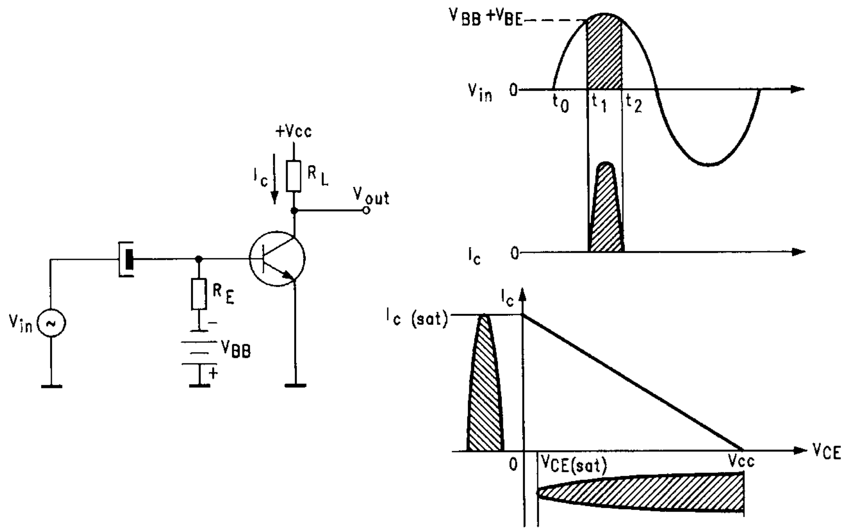


fig.B32.1

Operation

When a sine wave of voltage $v(t) = V_M \cdot \sin(\omega \cdot t)$, is connected to the input of the amplifier, the current $i(t)$ through the load R_L is different from zero in the conduction range $T = t_2 - t_1$, which corresponds to a conduction angle $\phi = \phi 2 - \phi 1$, where $\phi = \omega \cdot T$.

In a class C amplifier the angle ϕ is less than 180 degrees, and depends on the transistor bias.

The class C amplifier does not dissipate power in static conditions ($I_{CQ}=0$), while the power dissipated in dynamic conditions depends on the amplitude of the signal $v(t)$ and the conduction angle. For these reasons the efficiency of the class C amplifier is a function of the conduction angle ϕ; reducing this angle, the efficiency increases, and can take values approaching 100 %. Actually, we cannot reduce the conduction angle ϕ too much, because the overall power decreases too.

The train of pulses constituting the load current $i(t)$ represents a non-sinusoidal, periodic function. The period of this function equals the input signal period. Using a Fourier series, the load current can be represented by an infinite sum of sine waves :

$$i(t) = I_{CQ} + i_1 \cdot \sin(\omega \cdot t) + i_2 \cdot \sin(2 \cdot \omega \cdot t) + \ldots$$

If a resonant circuit is used as load, tuned at an harmonic of the fundamental, this amplifier can be used as frequency multiplier. Since the amplitude of the higher harmonics falls rapidly as frequency increases, the main amplification will be obtained at the fundamental frequency, i.e. at $f = \omega / 2 \cdot \pi$.

A class C amplifiers operate at very high efficiency, but is only used to amplify a single frequency. It cannot be used for the linear amplification. For these reasons, it is used with a resonant load to extract the main frequency, or possibly one of its harmonics.

B32.2 EXERCISES

➲ *MCM5*	**Disconnect all jumpers** **Set in OFF all S switches**
➲ *SIS1*	**Turn all switches *OFF***
➲ *SIS2*	**Insert lesson code: B32**

Amplifier with resistive load

- Set Vcc adjustable power supply to 12V.
- Insert jumpers J1, J3, J10, J11, J15, J17, J26, to produce the circuit of figure B32.2

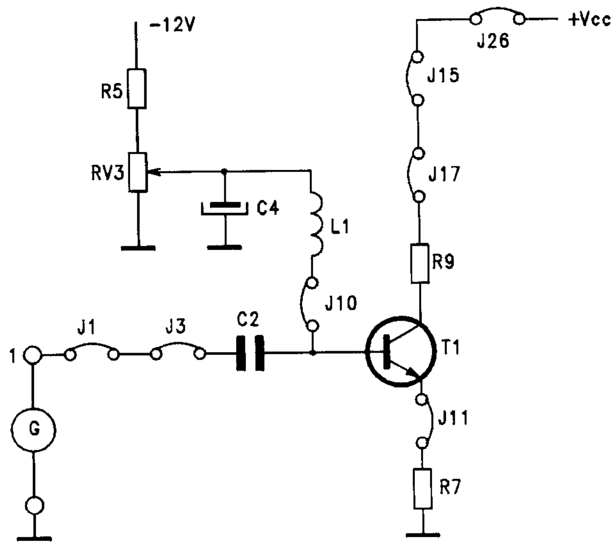


fig. B32.2

- adjust RV3, and consider how the bias voltage on the base of transistor T1 varies
- connect the function generator at terminals 1 and ground with a sine wave, 20 KHz and 1Vpp
- reduce the frequency of the input signal, and check the resulting signal on base of T1 with oscilloscope

Q1 *How does the amplitude vary with frequency?*

SET

A	*B*	
1	5	it remains constant
2	3	it is always zero
3	1	it decreases
4	2	it increases
5	4	it has a square-wave behavior

The inductance L1 separates the bias circuit, consisting of RV3 and R5, from the ac input signal. In fact the impedance of an inductance is proportional to frequency, so the higher the frequency, the higher will be reactance of L1, and the better will be the separation. The capacitor C4 is used to short-circuit any remaining signals across L1.

- adjust RV3 to set the voltage on the base of T1 to 0 V
- set the sine input signal to 20 KHz
- increase the amplitude of the input signal, observing the signal on the collector of T1 and across R7
- in particular, analyze the case in which the positive peak of the input voltage, applied across the base of T1, exceeds the threshold 0.6-0.7 V of the transistor

When the input voltage exceeds the transistor threshold voltage it starts conducting, generating small voltage pulses across the resistance R7. As the conduction angle is less smaller than 180 degrees, the amplifier is in class C

- adjust RV3 to negatively bias the base of T1 and check the behavior of the voltage across R7

Q2 *What happens to the output voltage on R7 as the base bias of T1 is continuously reduced?*

SET

A	*B*	
1	5	the peak amplitudes of the output signal increase
2	3	the amplitude of the output peaks decrease
3	1	the output signal frequency progressively increases
4	2	there is no output change
5	4	the phase shift between the input and output signal progressively increases

- vary RV3, and note the conduction angle of the output signal

Q3 *Comparing the conduction angles obtained with different bias conditions, we can say that:*

SET

A	*B*	
1	3	the conduction angle stays unchanged
2	1	the conduction angle increases when the voltage on the base of T1 decreases
3	2	the conduction angle decreases when the voltage on the base of T1 decreases

Tuned load

- Remove jumper J17 and insert J16, to produce the circuit of figure B32.3.
- adjust RV3 to obtain a base bias voltage of 0 V
- calculate the resonant frequency of the tuned circuit L2-C6, using the relation $fo = 1/(2 \cdot \pi \cdot \sqrt{L \cdot C})$, if L2 = 4μH and C6 = 680nF
- apply a sine signal of 2Vpp-amplitude and frequency fo to the input
- examine the wave-form of the signal across R7 (proportional to the current through the transistor) and also the signal on the collector
- adjust the input frequency to obtain the max. amplitude on the T1 collector (terminal 3)

When the frequency of the input signal is equal to the resonant frequency of the LC circuit, the output signal amplitude is max and the waveform is nearly distortionless. The amplifier is said to be tuned.

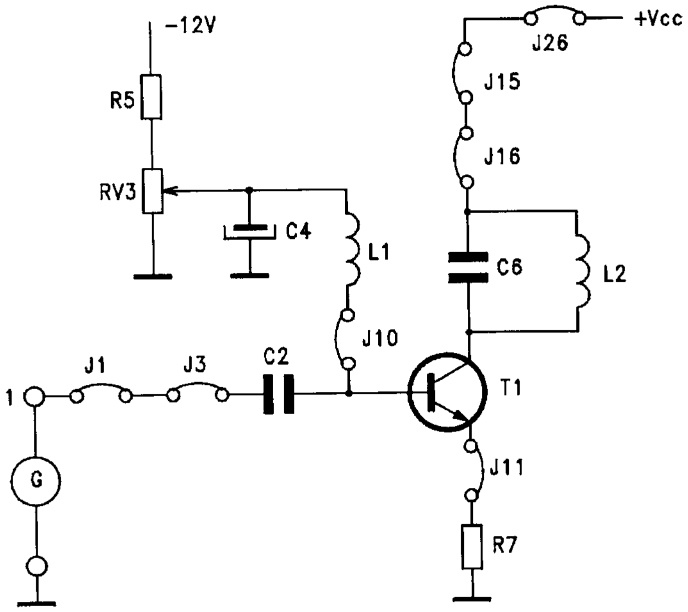


fig. B32.3

➲ *SIS1*	**Turn switch SW5 *ON***
➲ *SIS2*	**Press *INS***

Q4 *Noting the change in amplifier operation , we can say that:*

SET		
A	*B*	
1	3	the tuned output circuit has been changed
2	5	the base bias has been changed
3	4	the resistance R7 has been reduced
4	1	the power supply voltage VCC has been decreased
5	2	the transistor T1 has been short-circuited between base and collector

➲ *SIS1*	**Turn SW5 *OFF***

- slowly decrease the input signal frequency, until it is halved, while observing the behavior of the output signal on the T1 collector (terminal 3)
- in particular, analyze what happens when the input frequency gets near fo/2

As the frequency decreases, the amplitude of the output voltage slowly drops. If $fo/2 < f < fo$, the output has a behavior which is not sinusoidal anymore. Continuing to reduce the frequency, the second harmonic of the input signal clearly appears.

As the output frequency in this case is double the input signal frequency, the circuit can be used as frequency multiplier.

B32.3 SUMMARY QUESTIONS

Q5 *The operation in class C of an amplifier is characterized by conduction angles:*

SET

A	*B*	
1	5	greater than 180 degrees
2	1	equal to 180 degrees
3	2	less than 180 degrees
4	3	equal to 360 degrees
5	4	equal to 270 degrees

Q6 *Class C amplification produces a signal distortion which is :*

SET

A	*B*	
1	5	very small
2	1	very big
3	2	similar to the one produced by class A
4	3	similar to the one produced by class B
5	4	similar to the one produced by class AB

Q7 *The efficiency of a class C amplifier :*

SET

A	*B*	
1	2	depends on the conduction angle and takes very high values on average
2	1	is always very low
3	4	is always equal to 1
4	5	is close to 25 %
5	3	is equal to 50 %

Q8 *A tuned load in an amplifiers operating in class C can be used to produce:*

SET

A	*B*	
1	3	a frequency divider
2	1	a frequency multiplier
3	2	a half-wave rectifier
4	5	a voltage stabilizer
5	4	a current limiter

Appendix "A": SYMBOLS USED

The following points sum up the notation used for the voltages and currents.

1. The instantaneous values of the variables varying in time are represented with small letters ("v" for the voltage and "i" for the current)

2. the average value of the variables in time, or quantities which remain constant, are represented by the corresponding capital letters ("V" for the voltage and "I" for the current)

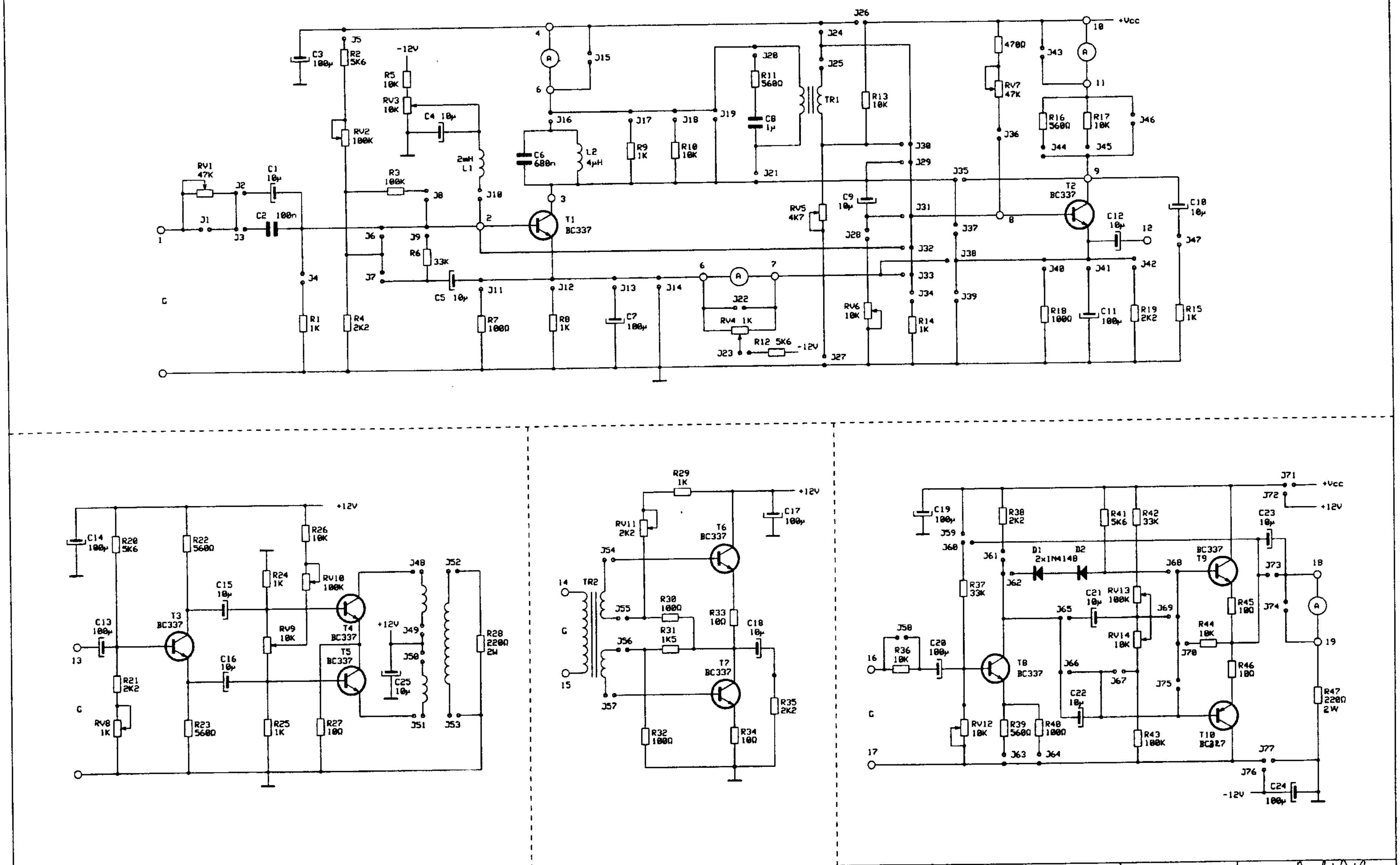
3. the terminals of a device are identified by the first capital letter of the name of the terminal (B=Base; D=Drain, etc.)

4. the currents in a device have an index letter corresponding to the terminal to which they refer to (e.g.: i_B, I_B, i_b, Base currents; i_D, I_D, i_d, Drain currents). The voltages between two terminals are identified by the indexes indicating those terminals (e.g.: v_{be}, v_{BE}, V_{BE}, - voltage between Base and Emitter)

5. the maximum value and the average value have the index in capitals (e.g.: i_B, I_B for the currents; v_{BE}, V_{BE} for the voltages)

6. the index for ac, or incremental components is in small letters (e.g.: i_b for the currents; v_{be} for the voltages).

7. the power supply voltage is usually indicated by repeating the capital index of the electrode to which it refers to, e.g. V_{CC} (although this symbol is sometimes used indiscriminately when the power is applied to other terminals, such as the Drain or Anode)



ELETTRONICA VENETA MOTTA DI LIVENZA - TV ITALY	DESCRIPTION : ELECTRONIC DEVICES AND CIRCUITS III EQUIPMENT : IPES MODULE MCM-5/EV T.C. FILE : -- SCALE : --	REPLACES: -- REPLACED BY: -- REVISION: 0	DWG Nº: MC051D01.FSH P.C.B.: MCM5 SHEET : 1 OF 1
			DRAWN : CHECKED : DATE : 09-01-97

Appendix “B”: DATA SHEETS

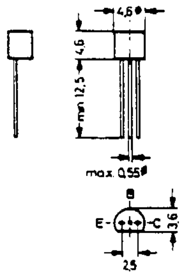
- **transistor NPN BC337**
- **transistor PNP BC327**

BC337, BC338

NPN Silicon Epitaxial Planar Transistors
for switching and amplifier applications. Especially suitable for AF-driver stages and low power output stages.

These types are also available subdivided into three groups -16, -25 and -40, according to their DC current gain. As complementary types the PNP transistors BC327 and BC328 are recommended.

On special request these transistors are also manufactured in the pinconfiguration TO-18.



Plastic package 10D3
according to DIN 41870 (≈ TO-92)
The case is impervious to light

Weight approximately 0.18 g
Dimensions in mm

Absolute Maximum Ratings

		Symbol	Value	Unit
Collector Emitter Voltage	**BC337** **BC338**	V_{CES} V_{CES}	50 30	V V
Collector Emitter Voltage	**BC337** **BC338**	V_{CEO} V_{CEO}	45 25	V V
Emitter Base Voltage		V_{EBO}	5	V
Collector Current		I_C	800	mA
Peak Collector Current		I_{CM}	1	A
Base Current		I_B	100	mA
Power Dissipation at T_{amb} = 25 °C		P_{tot}	625[1]	mW
Junction Temperature		T_j	150	°C
Storage Temperature Range		T_S	−55 to +150	°C

[1] Valid provided that leads are kept at ambient temperature at a distance of 2 mm from case

BC337, BC338

Characteristics at T_{amb} = 25 °C

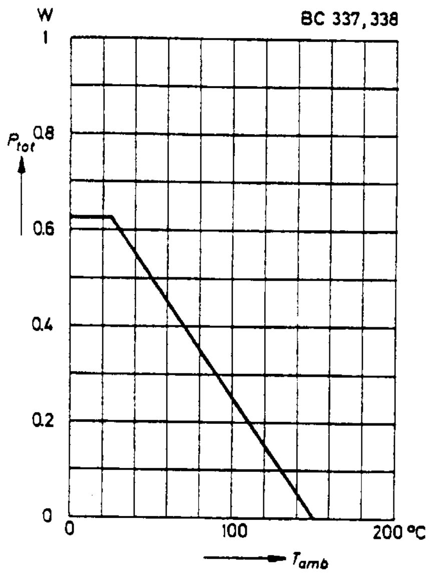
	Symbol	Min.	Typ.	Max.	Unit
DC Current Gain					
at V_{CE} = 1 V, I_C = 100 mA **BC337, BC338**	h_{FE}	100	–	630	–
Current Gain Group 16	h_{FE}	100	160	250	–
25	h_{FE}	160	250	400	–
40	h_{FE}	250	400	630	–
at V_{CE} = 1 V, I_C = 300 mA **BC337, BC338**	h_{FE}	60	–	–	–
Current Gain Group 16	h_{FE}	60	130	–	–
25	h_{FE}	100	200	–	–
40	h_{FE}	170	320	–	–
Collector Cutoff Current					
at V_{CE} = 25 V **BC338**	I_{CES}	–	2	100	nA
at V_{CE} = 45 V **BC337**	I_{CES}	–	2	100	nA
at V_{CE} = 25 V, T_{amb} = 125 °C **BC338**	I_{CES}	–	–	10	μA
at V_{CE} = 45 V, T_{amb} = 125 °C **BC337**	I_{CES}	–	–	10	μA
Collector Emitter Breakdown Voltage					
at I_C = 10 mA **BC338**	$V_{(BR)CEO}$	20	–	–	V
BC337	$V_{(BR)CEO}$	45	–	–	V
Collector Emitter Breakdown Voltage					
at I_C = 0.1 mA **BC338**	$V_{(BR)CES}$	30	–	–	V
BC337	$V_{(BR)CES}$	50	–	–	V
Emitter Base Breakdown Voltage at I_E = 0.1 mA	$V_{(BR)EBO}$	5	–	–	V
Collector Saturation Voltage at I_C = 500 mA, I_B = 50 mA	V_{CEsat}	–	–	0.7	V
Base Emitter Voltage at V_{CE} = 1 V, I_C = 300 mA	V_{BE}	–	–	1.2	V
Gain Bandwidth Product at V_{CE} = 5 V, I_C = 10 mA, f = 50 MHz	f_T	–	100	–	MHz
Collector Base Capacitance at V_{CB} = 10 V, f = 1 MHz	C_{CBO}	–	12	–	pF
Thermal Resistance Junction to Ambient	R_{thA}	–	–	200[1)]	K/W

[1)] Valid provided that leads are kept at ambient temperature at a distance of 2 mm from case

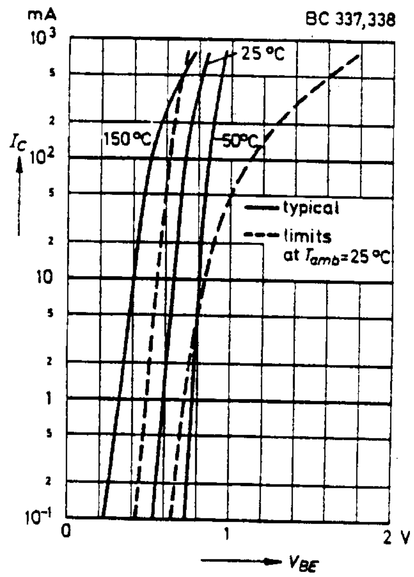
BC337, BC338

Admissible power dissipation versus ambient temperature

Valid provided that leads are kept at ambient temperature at a distance of 2 mm from case

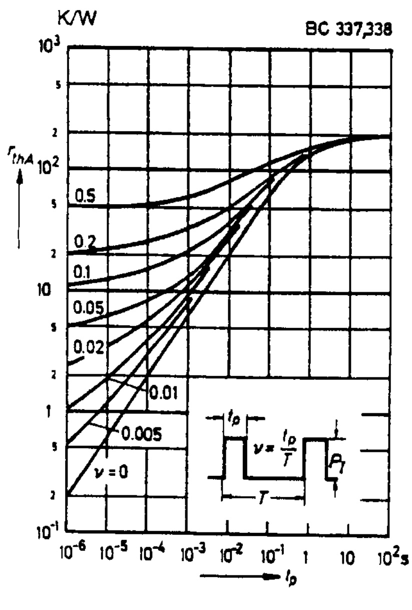


Collector current versus base emitter voltage

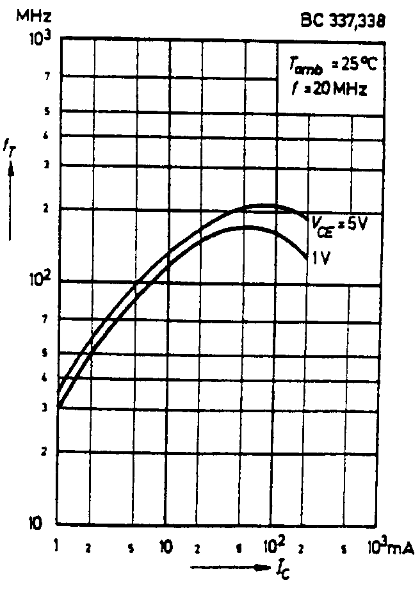


Pulse thermal resistance versus pulse duration

Valid provided that leads are kept at ambient temperature a a distance of 2 mm from case

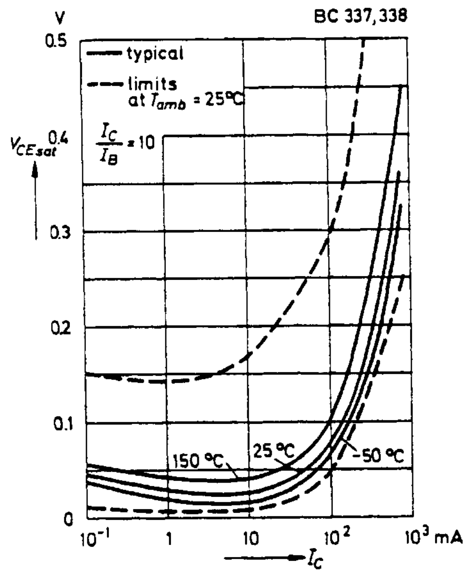


Gain bandwidth product versus collector current

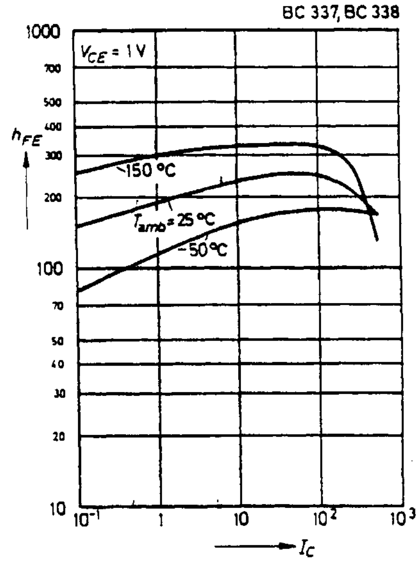


BC 337, BC338

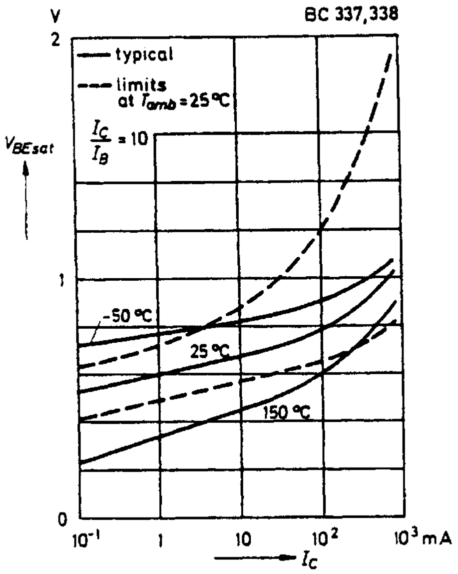
Collector saturation voltage versus collector current



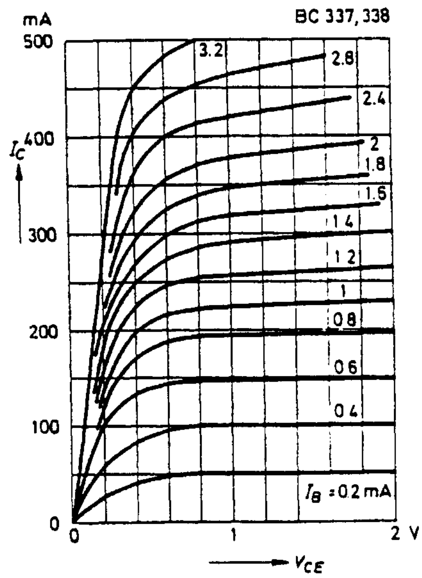
DC current gain versus collector current



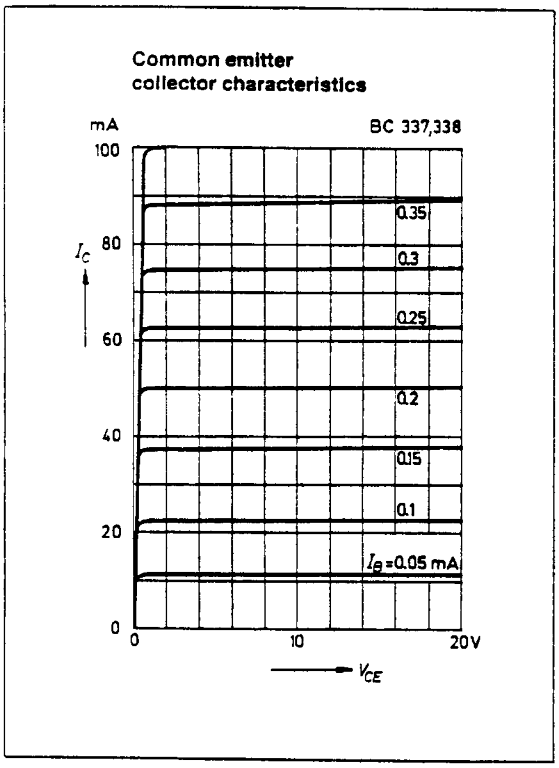
Base saturation voltage versus collector current

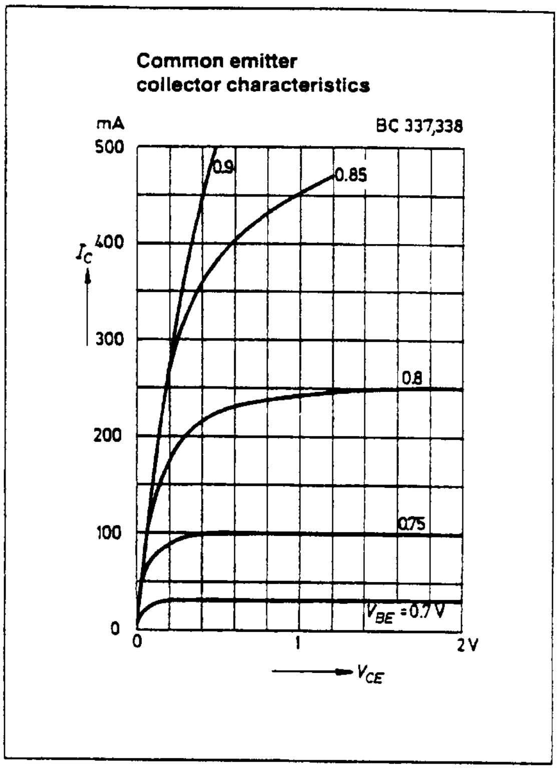


Common emitter collector characteristics



BC337, BC338


Common emitter
collector characteristics
mA
BC 337,338
100
80
60
40
20
0
I_C
0.35
0.3
0.25
0.2
0.15
0.1
I_B = 0.05 mA
0
10
20V
V_{CE}

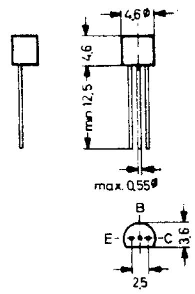

Common emitter
collector characteristics
mA
BC 337,338
500
400
300
200
100
0
I_C
0.9
0.85
0.8
0.75
V_{BE} = 0.7 V
0
1
2V
V_{CE}

BC327, BC328

PNP Silicon Epitaxial Planar Transistors
for switching and amplifier applications. Especially suitable for AF-driver stages and low power output stages.

These types are also available subdivided into three groups −16, −25 and −40, according to their DC current gain. As complementary types the NPN transistors BC337 and BC338 are recommended.

On special request these transistors are also manufactured in the pinconfiguration TO-18.



Plastic package 10D3
according to DIN 41870 (≈ TO-92)
The case is impervious to light

Weight approximately 0.18 g
Dimensions in mm

Absolute Maximum Ratings

	Symbol	Value	Unit
Collector Emitter Voltage **BC327**	$-V_{CES}$	50	V
BC328	$-V_{CES}$	30	V
Collector Emitter Voltage **BC327**	$-V_{CEO}$	45	V
BC328	$-V_{CEO}$	25	V
Emitter Base Voltage	$-V_{EBO}$	5	V
Collector Current	$-I_C$	800	mA
Peak Collector Current	$-I_{CM}$	1	A
Base Current	$-I_B$	100	mA
Power Dissipation at T_{amb} = 25 °C	P_{tot}	625[1)]	mW
Junction Temperature	T_j	150	°C
Storage Temperature Range	T_S	−55 ... +150	°C

[1)] Valid provided that leads are kept at ambient temperature at a distance of 2 mm from case

BC327, BC328

Characteristics at $T_{amb} = 25\ °C$

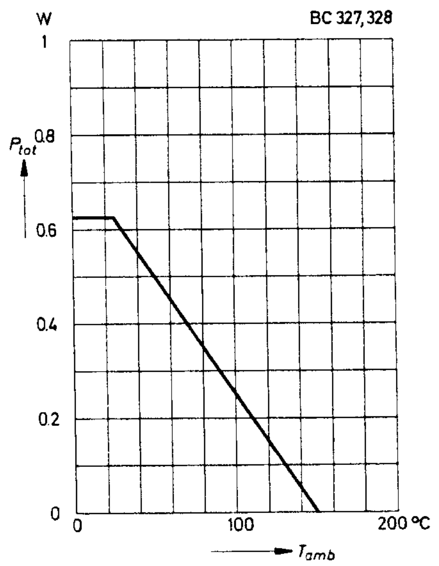
	Symbol	Min.	Typ.	Max.	Unit
DC Current Gain					
at $-V_{CE} = 1$ V, $-I_C = 100$ mA **BC327, BC328**	h_{FE}	100	–	630	–
Current Gain Group 16	h_{FE}	100	160	250	–
25	h_{FE}	160	250	400	–
40	h_{FE}	250	400	630	–
at $-V_{CE} = 1$ V, $-I_C = 300$ mA **BC327, BC328**	h_{FE}	60	–	–	–
Current Gain Group 16	h_{FE}	60	130	–	–
25	h_{FE}	100	200	–	–
40	h_{FE}	170	320	–	–
Thermal Resistance Junction to Ambient	R_{thA}	–	–	200[1]	K/W
Collector Cutoff Current					
at $-V_{CE} = 25$ V **BC328**	$-I_{CES}$	–	2	100	nA
at $-V_{CE} = 45$ V **BC327**	$-I_{CES}$	–	2	100	nA
at $-V_{CE} = 25$ V, $T_{amb} = 125\ °C$ **BC328**	$-I_{CES}$	–	–	10	μA
at $-V_{CE} = 45$ V, $T_{amb} = 125\ °C$ **BC327**	$-I_{CES}$	–	–	10	μA
Collector Emitter Breakdown Voltage					
at $-I_C = 10$ mA **BC327**	$-V_{(BR)CEO}$	45	–	–	V
BC328	$-V_{(BR)CEO}$	25	–	–	V
Collector Emitter Breakdown Voltage					
at $-I_C = 0.1$ mA **BC327**	$-V_{(BR)CES}$	50	–	–	V
BC328	$-V_{(BR)CES}$	30	–	–	V
Emitter Base Breakdown Voltage at $-I_E = 0.1$ mA	$-V_{(BR)EBO}$	5	–	–	V
Collector Saturation Voltage at $-I_C = 500$mA, $-I_B = 50$ mA	$-V_{CEsat}$	–	–	0.7	V
Base Emitter Voltage at $-V_{CE} = 1$V, $-I_C = 300$ mA	$-V_{BE}$	–	–	1.2	V
Gain Bandwidth Product at $-V_{CE} = 5$ V, $-I_C = 10$ mA, f = 50 MHz	f_T	–	100	–	MHz
Collector Base Capacitance at $-V_{CB} = 10$ V, f = 1 MHz	C_{CBO}	–	12	–	pF

[1] Valid provided that leads are kept at ambient temperature at a distance of 2 mm from case

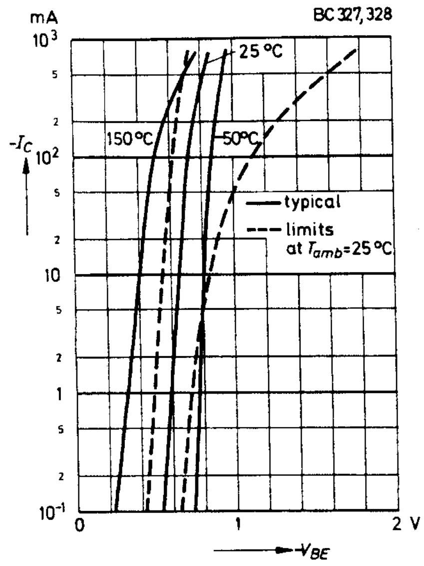
BC327, BC328

Admissible power dissipation versus ambient temperature

Valid provided that leads are kept at ambient temperature at a distance of 2 mm from case

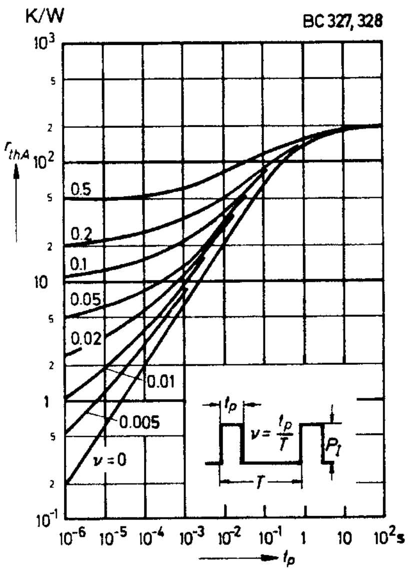


Collector current versus base emitter voltage

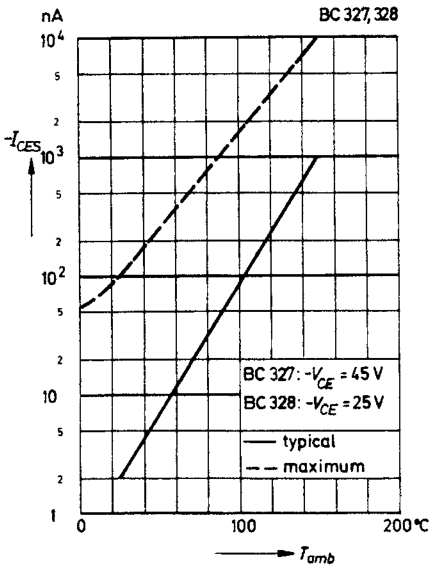


Pulse thermal resistance versus pulse duration

Valid provided that leads are kept at ambient temperature at a distance of 2 mm from case

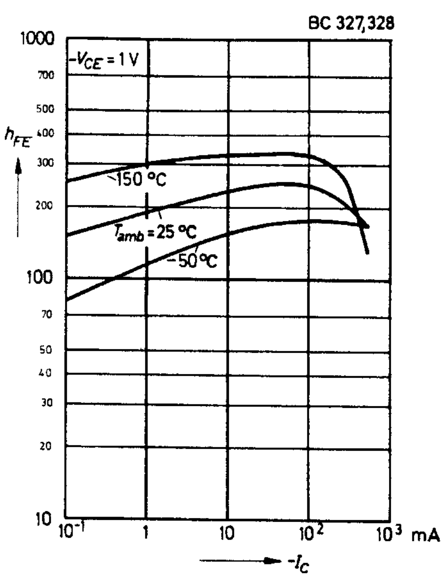


Collector cutoff current versus ambient temperature

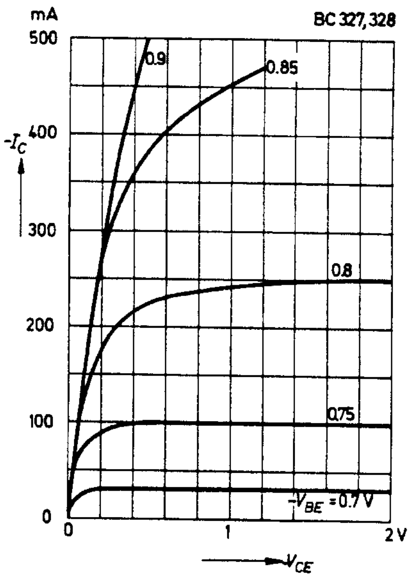


BC327, BC328

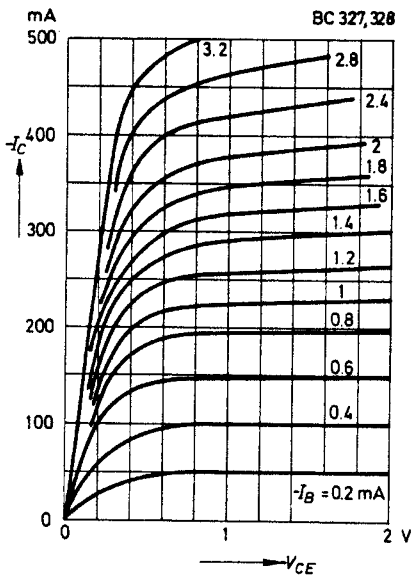
DC current gain versus collector current



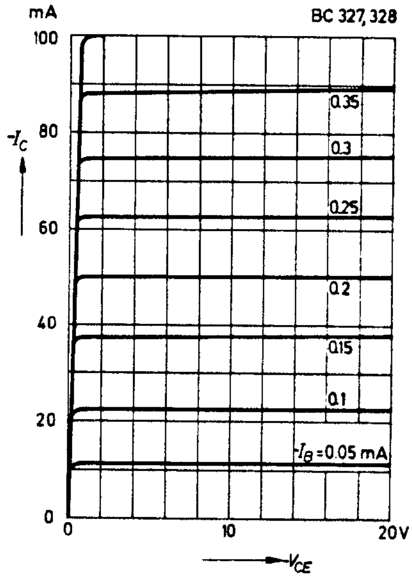
Common emitter collector characteristics



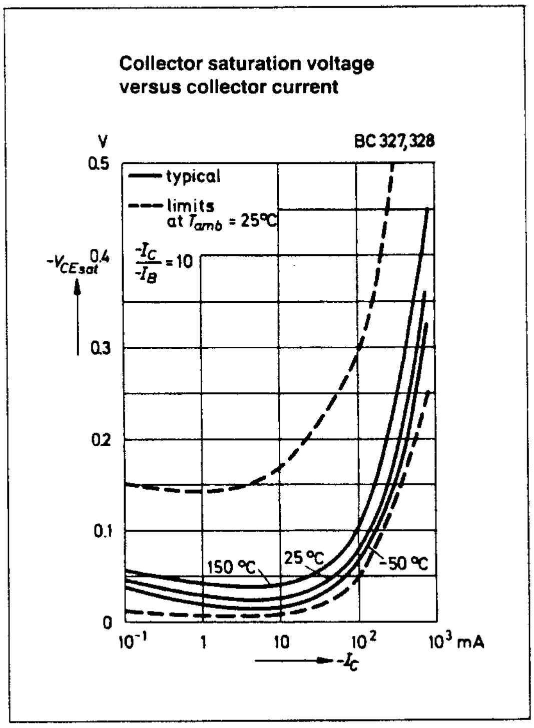
Common emitter collector characteristics

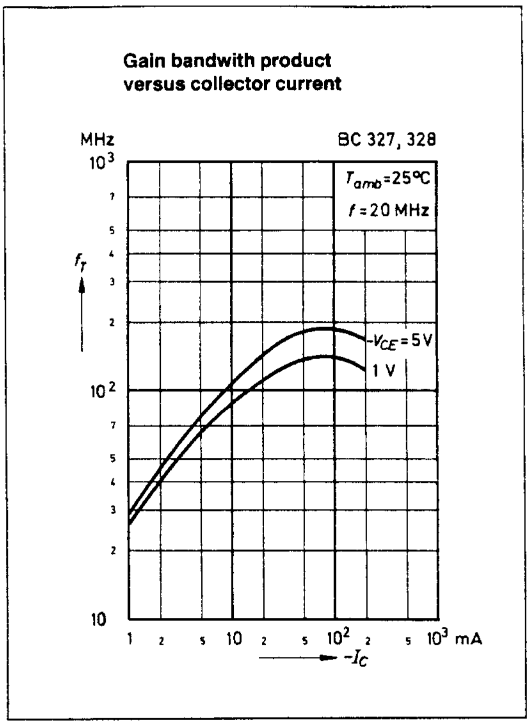


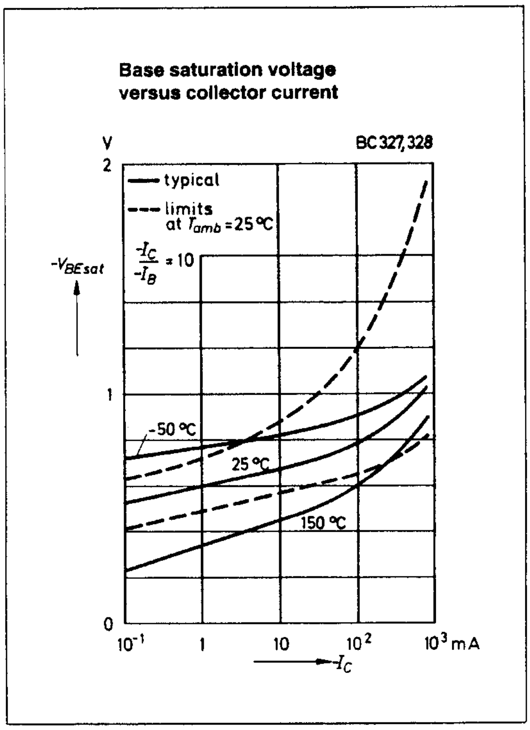
Common emitter collector characteristics



BC327, BC328


Collector saturation voltage
versus collector current
BC 327,328
typical
limits
at T_{amb} = 25°C
$\frac{-I_C}{-I_B}$ = 10
$-V_{CEsat}$
V
0.5
0.4
0.3
0.2
0.1
0
150 °C
25 °C
-50 °C
10^{-1}
1
10
10^2
10^3 mA
$-I_C$


Gain bandwith product
versus collector current
BC 327, 328
MHz
10^3
10^2
10
f_T
T_{amb}=25°C
f = 20 MHz
$-V_{CE}$ = 5 V
1 V
1
10
10^2
10^3 mA
$-I_C$


Base saturation voltage
versus collector current
BC 327,328
typical
limits
at T_{amb} = 25°C
$\frac{-I_C}{-I_B}$ = 10
$-V_{BEsat}$
V
2
1
0
-50 °C
25 °C
150 °C
10^{-1}
1
10
10^2
10^3 mA
$-I_C$

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