# The analysis of the linear voltage regulators

**1. Theoretical aspects**

The voltage regulator is an electronic circuit which, ideally, it provides a constant output voltage. The value of the output voltage should not depend on parameters such as: the supply voltage of the regulator, the ambient temperature, the output current through the load. Actually, the output voltage is influenced by these parameters, but its variation can be controlled and minimized by careful design. The most important parameters that characterize a voltage regulator are:

- The output voltage ($V_o$) which should be a constant;
- The output resistance ($R_o$) which should be as small as possible (0Ω).

Some of the physical quantities that define the voltage regulator dependence on the influences of the external environment are:

- the minimum ($V_{imin}$) and the maximum ($V_{imax}$) supply voltages;
- the maximum output current ( $I_{omax}$);
- The line regulation $S = \left.\frac{\Delta V_i}{\Delta V_o}\right|_{R_L = given}$ ;
- The load regulation is the change in output voltage for a given change in load current;
- The temperature coefficient of the output voltage is the change of the output voltage with temperature.

The voltage regulators described in this paper are using the integrated circuit LM723 (ßA723). The IC has the block diagram represented in Fig.1.

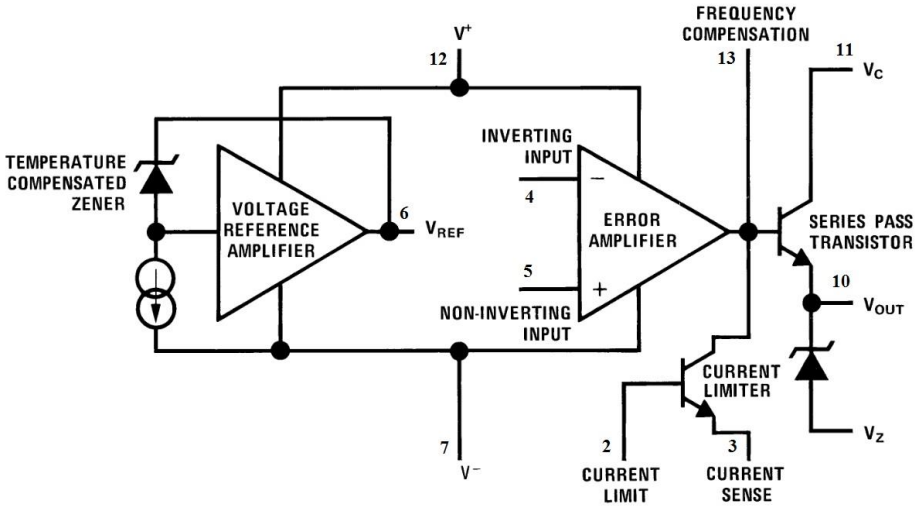


**Fig.1. The internal structure of the integrated circuit LM723**

The simulation is performed at two different output voltages: $V_o<V_{REF}$ , and $V_o>V_{REF}$ respectively. For the first case ($V_o<V_{REF}$ ), the simplified equivalent circuit of the voltage regulator is presented in Fig.2. By considering an ideal error amplifier (AE), the output voltage is:

$$V_o = \frac{R_2}{R_1 + R_2} \cdot V_R \quad (1)$$

For the given circuit, the error amplifier fulfills the task of a voltage buffer (its voltage gain is 1).

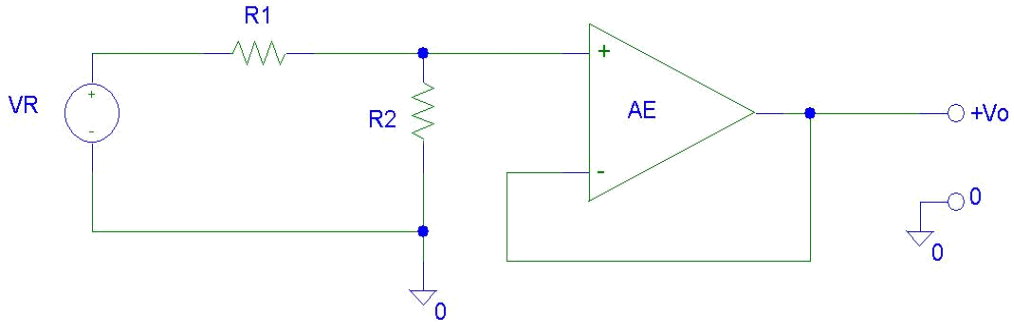


**Fig.2. The block diagram of the voltage regulator with $V_o<V_{REF}$**

For higher values of the output voltage ($V_o>V_{REF}$ ), the simplified block diagram of the voltage regulator is given is Fig.3.

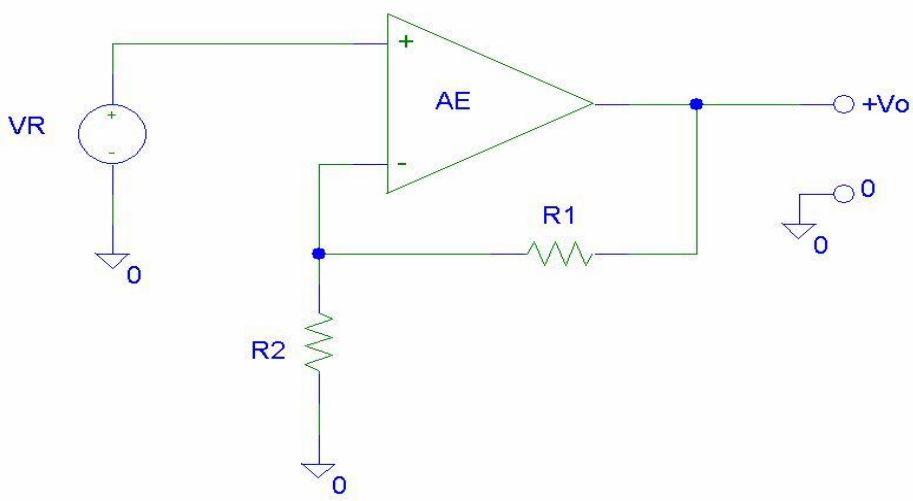


**Fig.3. The block diagram of the voltage regulator with $V_o>V_{REF}$**

The output voltage is:

$$V_o = \frac{R_1 + R_2}{R_2} \cdot V_R$$

The schematic diagram of the voltage regulator with low output voltages ($V_o<V_R$) is represented in Fig.4.

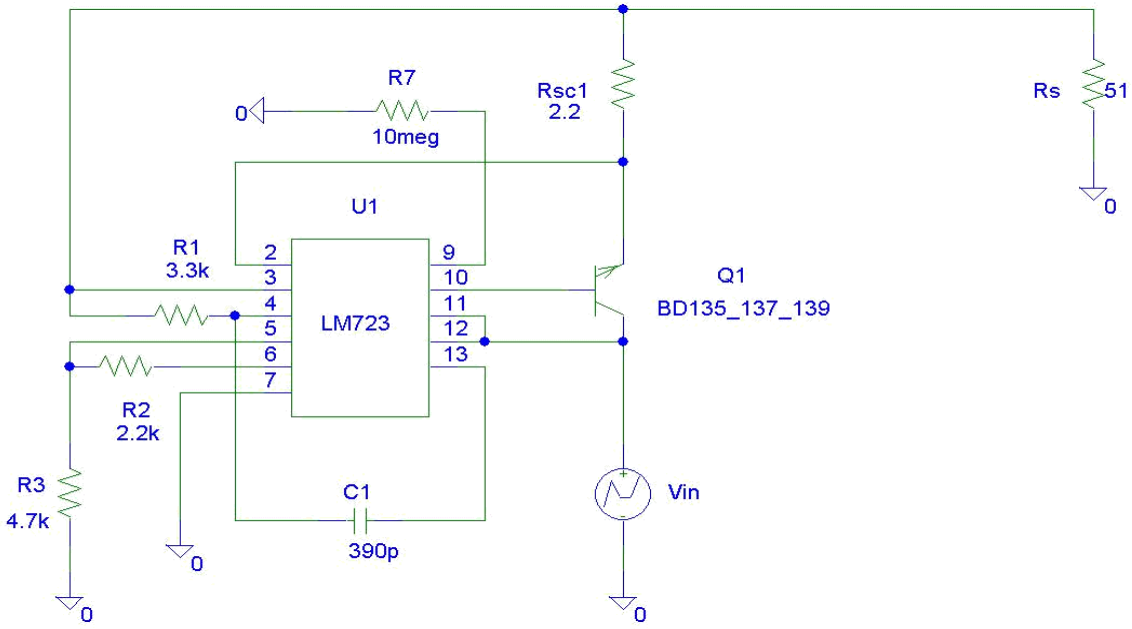


**Fig 4. The schematic diagram of the voltage regulator for small output voltages $V_o<V_R$**

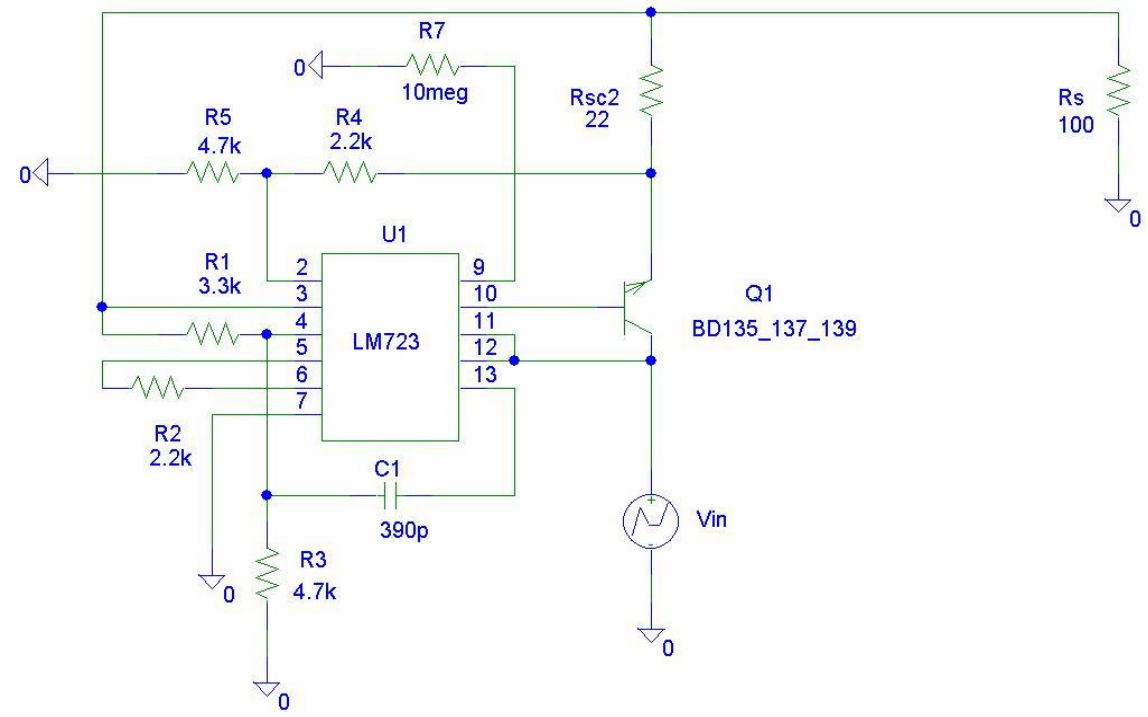


**Fig 5. The schematic diagram of the voltage regulator for high output voltages $V_0 > V_R$**

*Table 1*

| Name | Component | Value | Library |
|---|---|---|---|
| Vin | VPWL | T1=0 ; V1=0; T2=1; V2=1; T3=10; V3=20 | Source.slb |
| Rx ( x=1…n ) | R | - only the numerical value for ohms range<br>- for kilo ohms range a "k" should be placed after the numerical value (no space between characters) | Analog.slb |
| Cx (x=1…n ) | C | - For picofarads range: a p should be placed immediately after the numerical value<br>- For nanofarads range: a n should be placed immediately after the numerical value<br>- For microfarads range: a u should be placed immediately after the numerical value | Analog.slb |
| U1 | LM723 | Linear voltage regulator | Stab.slb |
| $R_s$ | R_var | Variable resistor | Analog.slb |
| $Q_1$ | BD135_137_139 | Medium power NPN bipolar junction transistor | Stab.slb |
| Ground | GND_ANALOG | 0 | Port.slb |

The schematic is draw by using the "Schematics" editor from the "Pspice Student 9.1" software package provided by the Cadence Company free of charge. The components may be placed on the schematic by using the "Draw - Get New Part ..." command (CTRL + G). The components may be rotated by using the "Edit-Rotate" command (CTRL + R). The components may be put into a mirror by using the "Edit-Flip" command (CTRL + F).

After the convenient positioning of the components on the schematic, the connections are made by using the "Draw-Wire" (CTRL + W) command and the mouse. The components used to draw the schematics are listed in Table 1.

When the schematic has been drawn and saved (CTRL + S command), a circuit simulation should be accomplished by selecting the "Analysis-Setup ..." and choosing a time domain simulation for 20s ("Transient ...", "Final time = 20s", Fig.6).

To draw the Vo(Vin) characteristic, the default parameter on X axis (time) should be replaced by the circuit supply voltage (Vin). In the Pspice A / D menu, select "Plot-Axis Settings" and choose "Axis Variable ..." as V1(Vin) (Fig. 7).

To represent the output voltage according to the input voltage, we will use the "Trace-Add Trace" (INSERT) command and we will choose the parameter V2(Rs) on Y-axis (Fig. 8).

After selecting the simulation parameters, the cursor is placed on the graph ("Trace-Cursor-Display") (Toggle Cursor) to read the linear regulator output voltage Vo(Vin) (Fig.9).

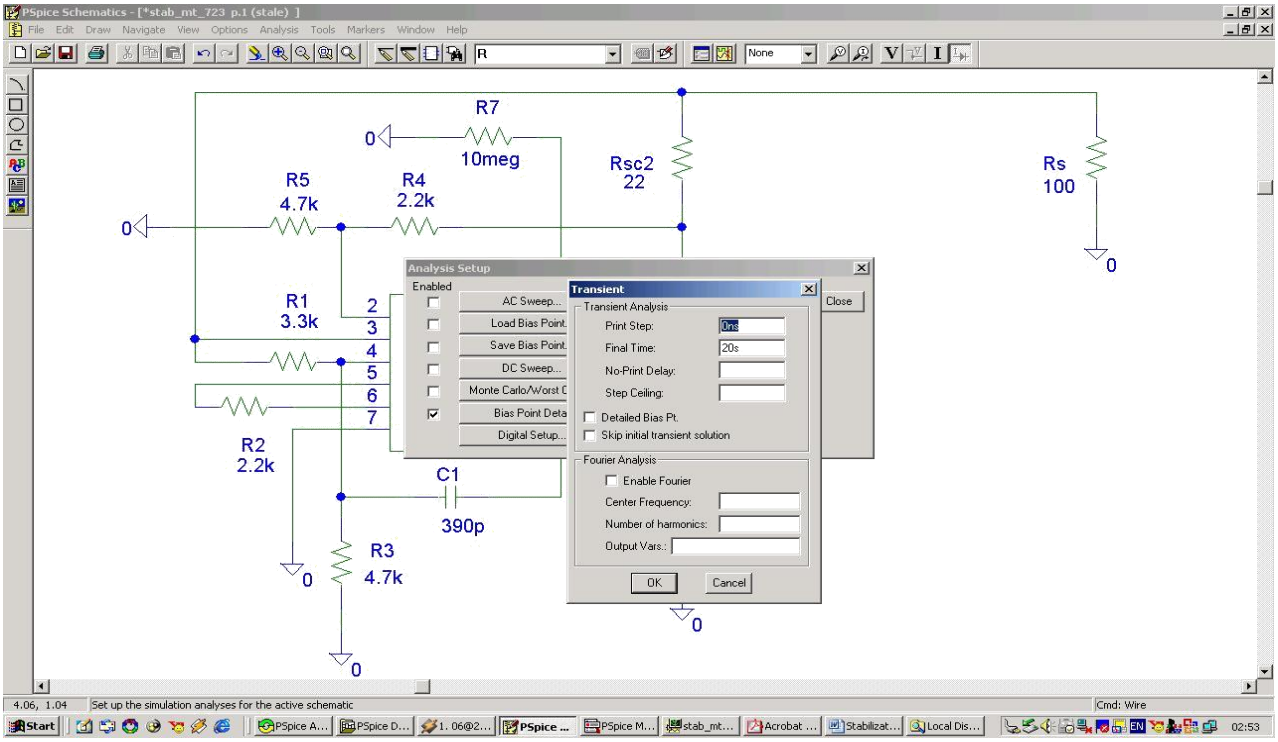


**Fig.6.The selection of the time domain simulation**

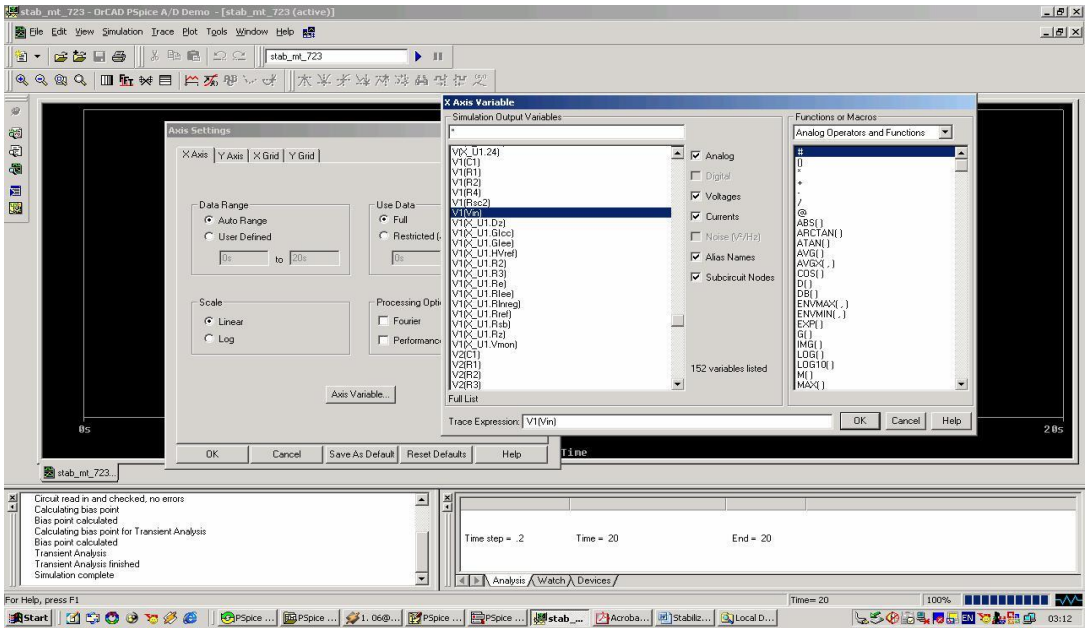


**Fig.7. Setting the Vin parameter on X axis**

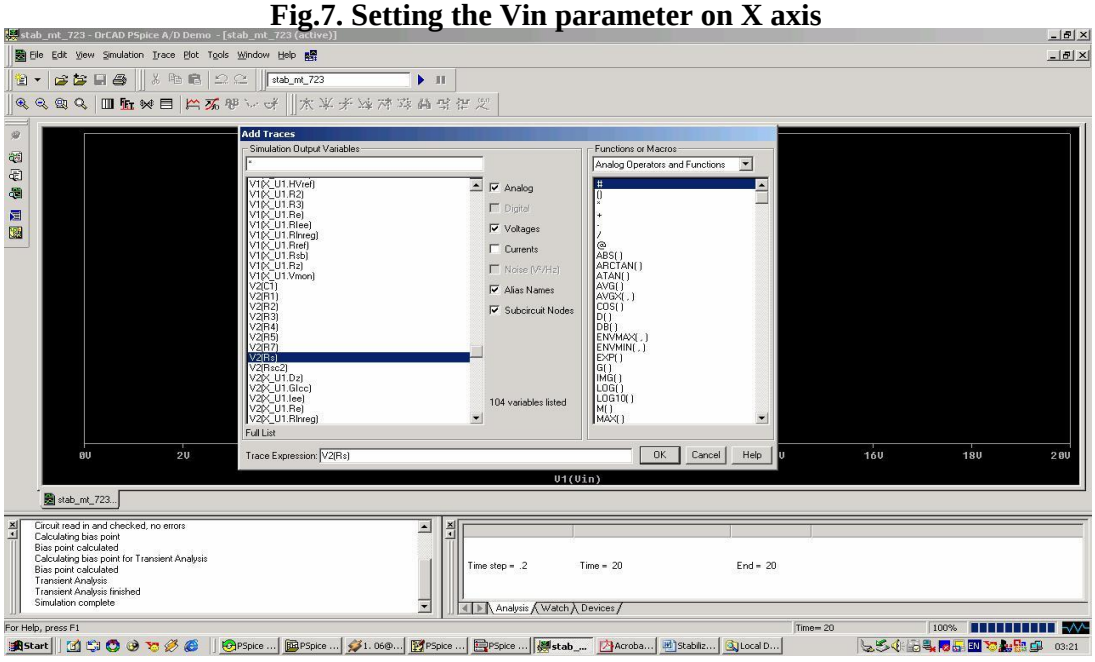


**Fig8. Setting the output voltage parameter on Y axis**

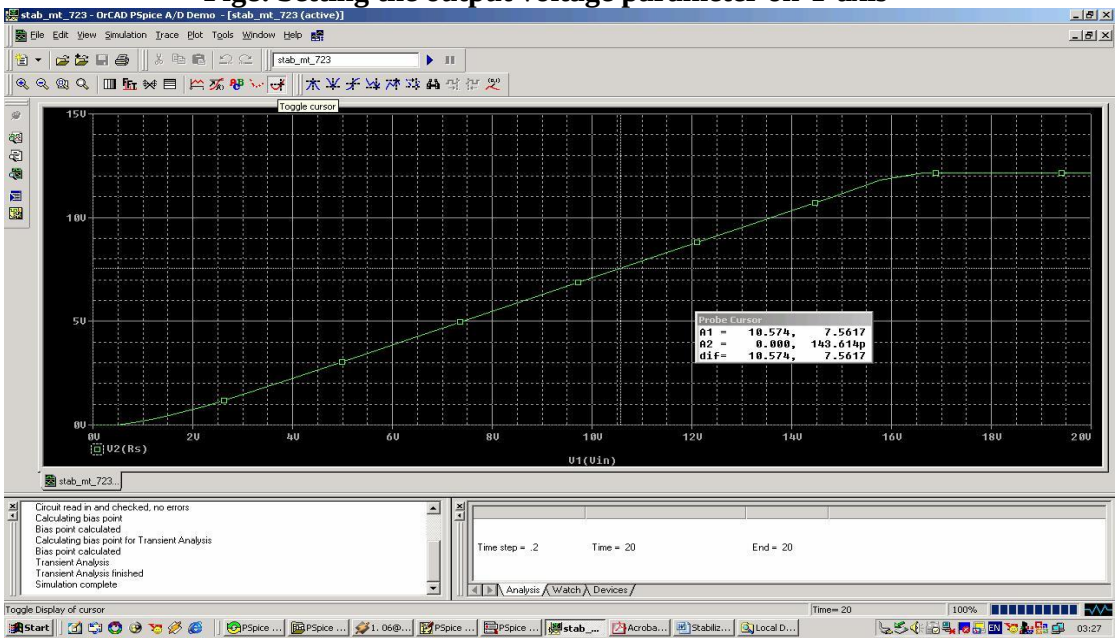


**Fig.9.The transfer characteristic of the linear voltage regulator ($V_o(V_{in})$)**

## 2. Laboratory work

1. Draw the circuit diagram of the linear voltage regulator with $V_O < V_R$(Fig. 4).
   A. The load value is Rs = 51Ω;
   B. A time domain simulation should be selected. The graphic representation of the Vo(Vin) is done by replacing the time on the X axis by $V_{in}$. Determine the minimum supply voltage ($V_{inmin}$) to obtain a constant output voltage ($V_o$). This is the minimum supply voltage from which the voltage regulator works properly.
2. Draw the schematic from Fig. 10, and put the $V_S$ parameters: VPWL, with T1=0, V1=0, T2=10, V2=4.8. The simulation time should be set at 20s.

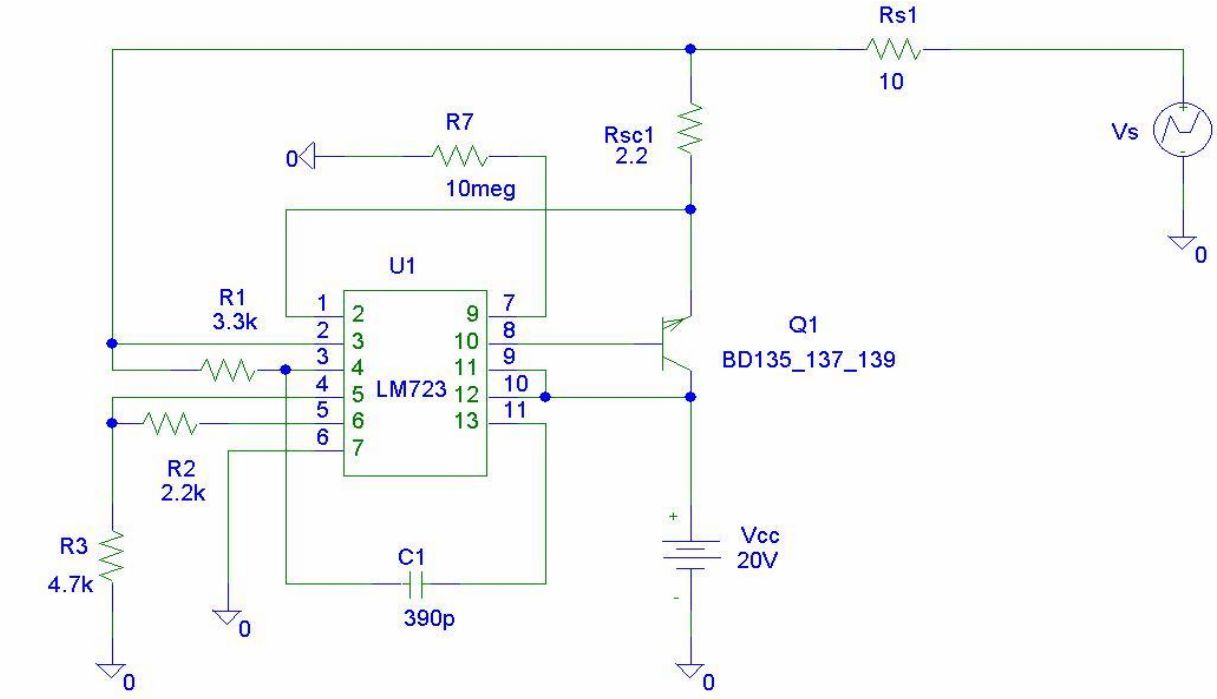


**Fig.10. The circuit for the simulation of the output characteristic ($V_o$ –$I_o$)**

After running the simulation (F11), the parameter on X axis is set to be the current through the load: "Plot-Axis Settings ... -X Axis-Axis Variable ... - I (Rs1)". The output voltage versus the output current is represented by using"Trace-Add Trace-V (U1: 3) -OK" as shown in Fig.11. It is required to determine:

A. the maximum output current value Io for which the output voltage Vo is stable (Iomax)
B. the power dissipated on the transistor Q1 for Io = Iomax and Vs = 0 (Rs = 10Ω).
C. Which is the hardest operating regime for the Q1 transistor?

3. Draw the electrical diagram of the linear voltage stabilizer with Vo> VR and over current protection(Fig.5).

A. Set RS = 51Ω;

B. Do the simulation of Vo (Vin) charactersitic and determine the minimum value of the $V_{imin}$ supply voltage from which the output voltage (Vo) remains constant. This value is the minimum input voltage required for the regulator to work properly.

4. Modify the circuit in Fig.5 by replacing the variable power supply (Vin) with a fixed voltage source Vcc (VDC=20V). Replace the load with a variable resistor R_var (named Rs1) (Fig.12).

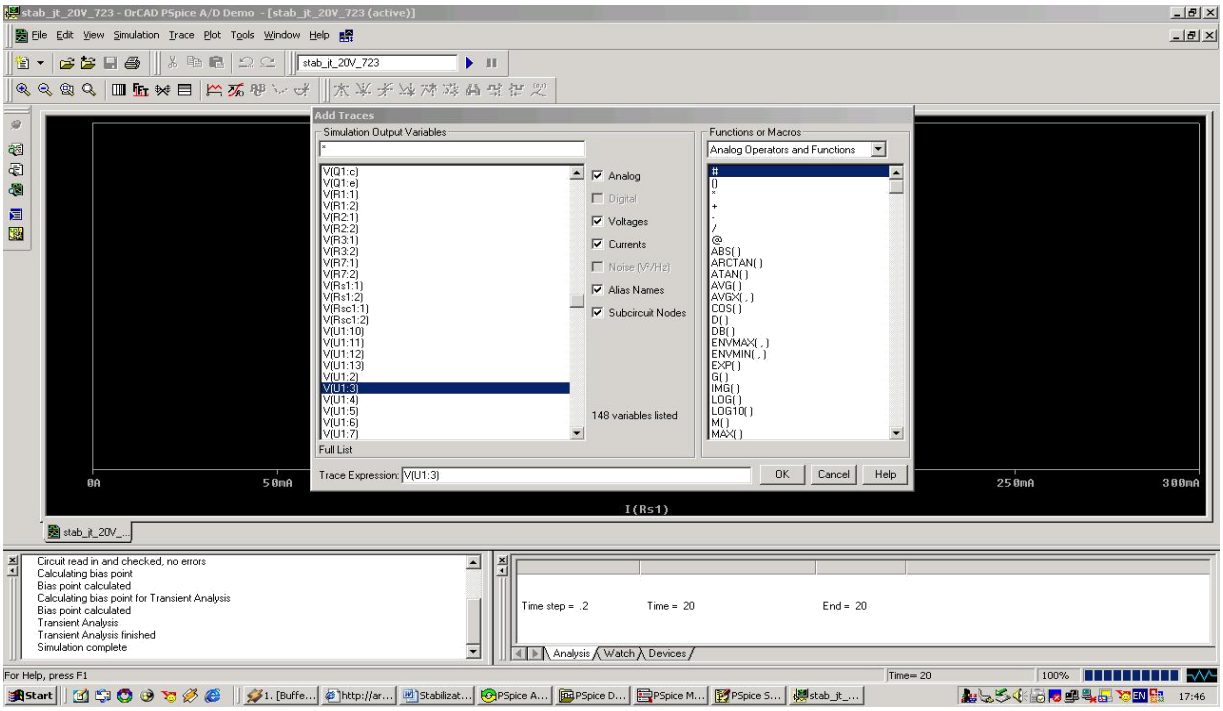


**Fig. 11. The $V_o$-$I_o$ characteristic**

By changing the SET parameter, the cursor of the potentiometer R_var is positioned, changing its value and implicitly the current absorbed by the load. The relationship between the position of the cursor and the resistance value is given by:

$$R\_\text{var} = \frac{SET}{R\_\text{var\_max}}$$

, where $R_{var\_max}$=201Ω. The SET parameter may be calculated for each corresponding value of R-_var in Table 2. After the simuation is accomplished, the "Bias point detail" and "Enable Bias Voltage Display" (" Analysis-Display results on schematic- Enable voltage display") options should be selected to permit the display of the continuous DC voltages in the nodes of the circuit.

*Table 2*

| R_var (Ω ) | 201 | 153 | 76.5 | 51 | 42.5 | 31 | 25.5 | 10.2 | 0 |
|---|---|---|---|---|---|---|---|---|---|
| $V_o$(V) | | | | | | | | | |
| $I_o$=$V_o$/R_var | | | | | | | | | |
| $V_{E1}$ (V) | | | | | | | | | |
| $V_{CE1}$ | | | | | | | | | |

The $V_{E1}$ is the potential of the emitter of Q1 BJT (V(Q1:e) ). The $V_{CE1}$ is the collector-emitter voltage for the Q1 transistor (V(Q1:c) - V(Q1:e) ).

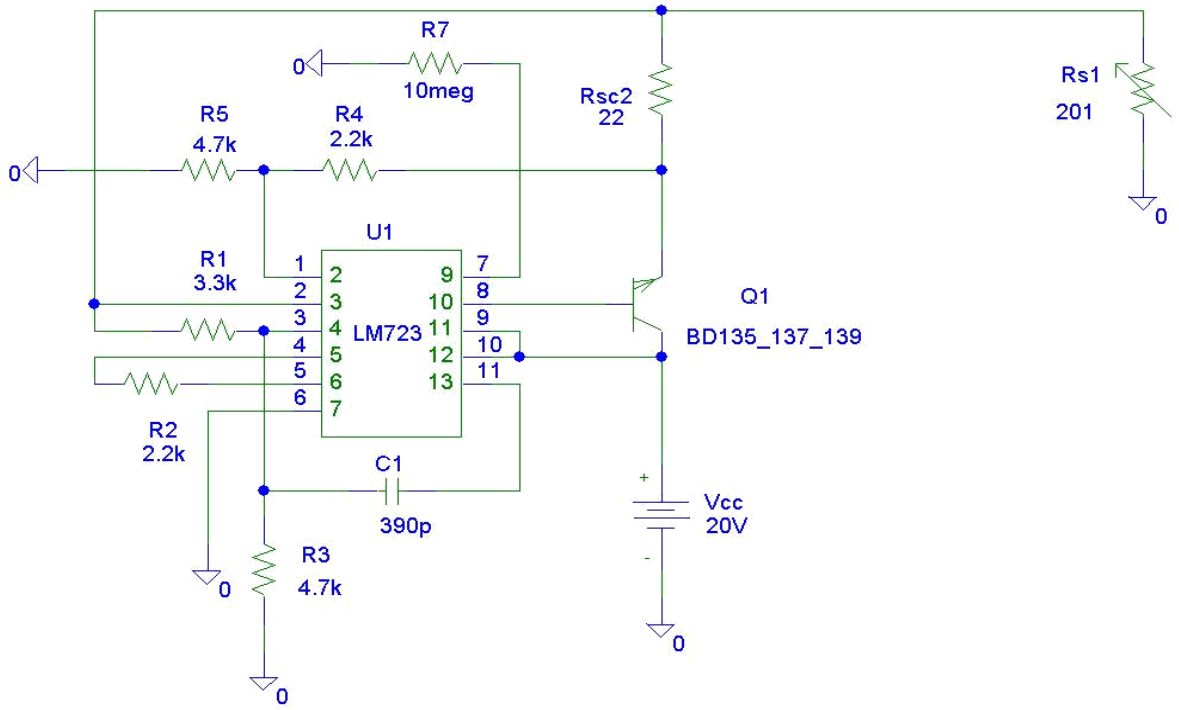


**Fig.12. The voltage regulator schematic with R_var and $V_o > V_R$**

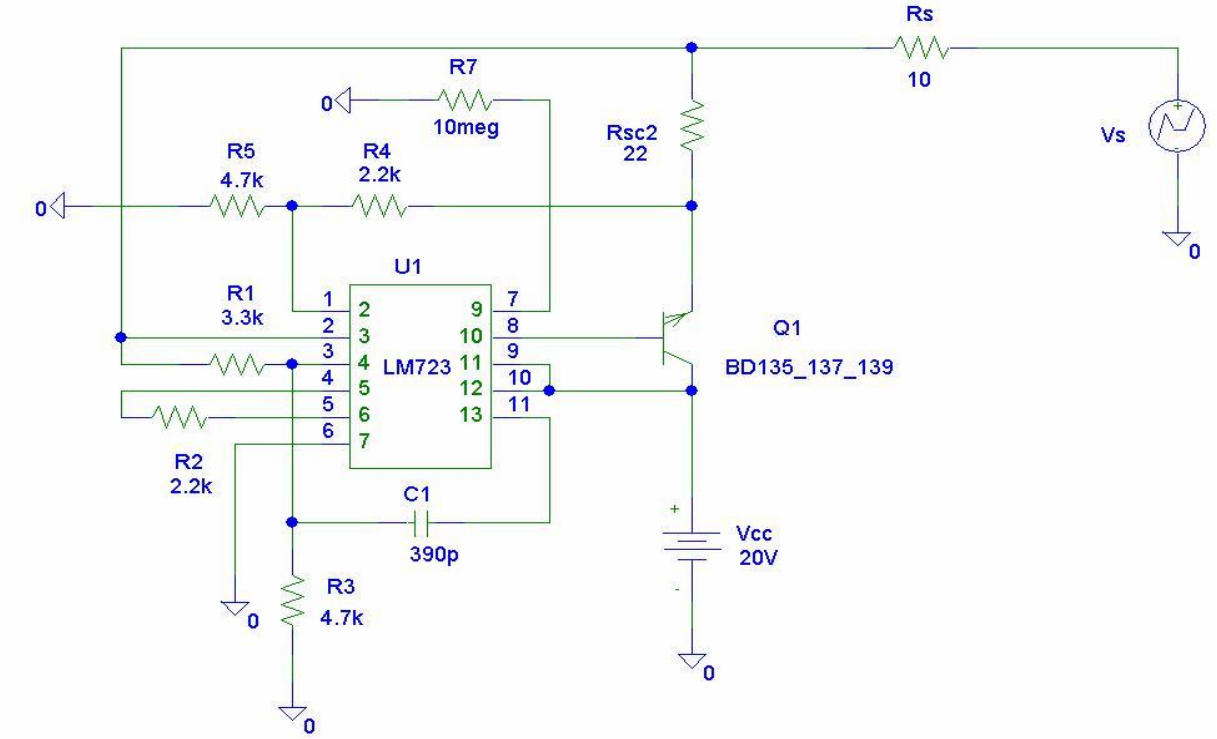


**Fig.13. The circuit used to simulate the $V_o(I_o)$ characteristic for $V_o > V_R$ situation**

5. The load of the voltage regulator is replaced by a fixed resistor in series with a variable voltage source $V_S$. The $V_S$ will be a VPWL type with the following parameters: T1=10, V1=0; T2=10, V2=12. The simulation time will be set to 20s (Fig.14).

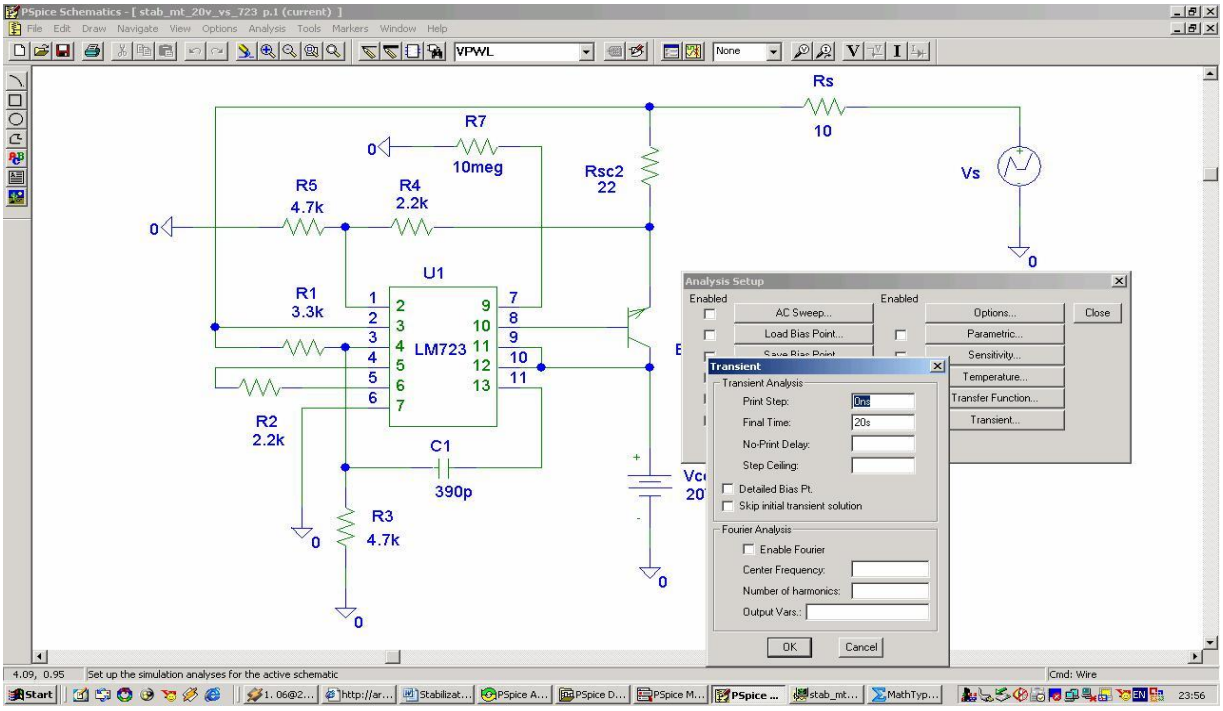


**Fig.14. Setting the simulation time for $V_o$>$V_R$ case**

After the simulation has ended, the output current $I_o$ is represented on X axis: "Plot-Axis Settings- X axis- Axis Variable… I(Rs)":

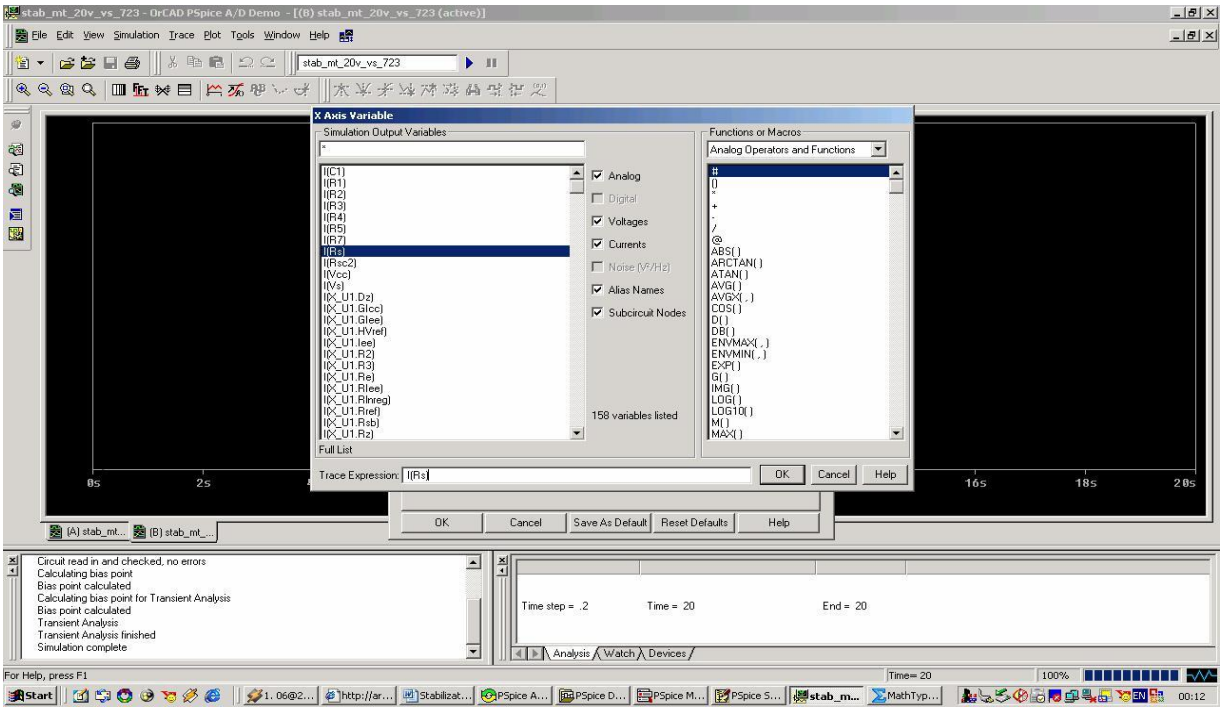


**Fig.15. Representing the output current on X axis**

Then, the output voltage ($V_o$) is displayed on Y axis :V(U1:3) (Fig.16).

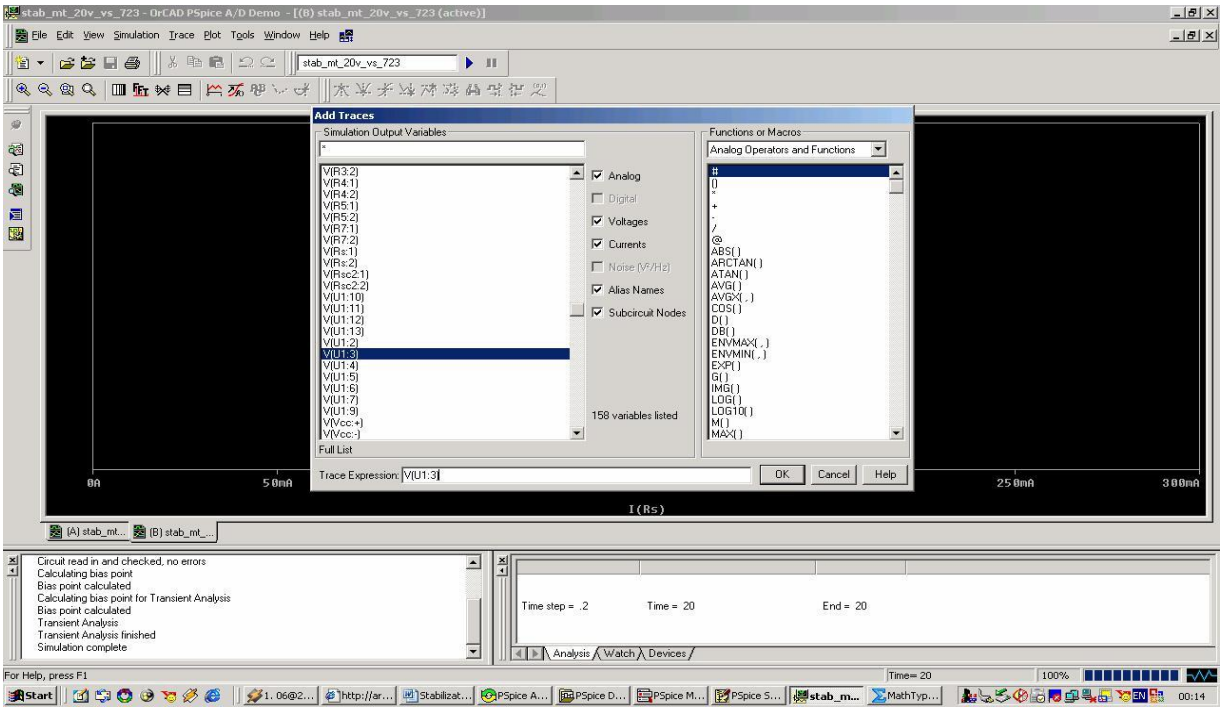


**Fig.16. Selecting the output voltage to be displayed for $V_o$>$V_R$ case**

The values on the graph may be read by using the Toggle Cursor:

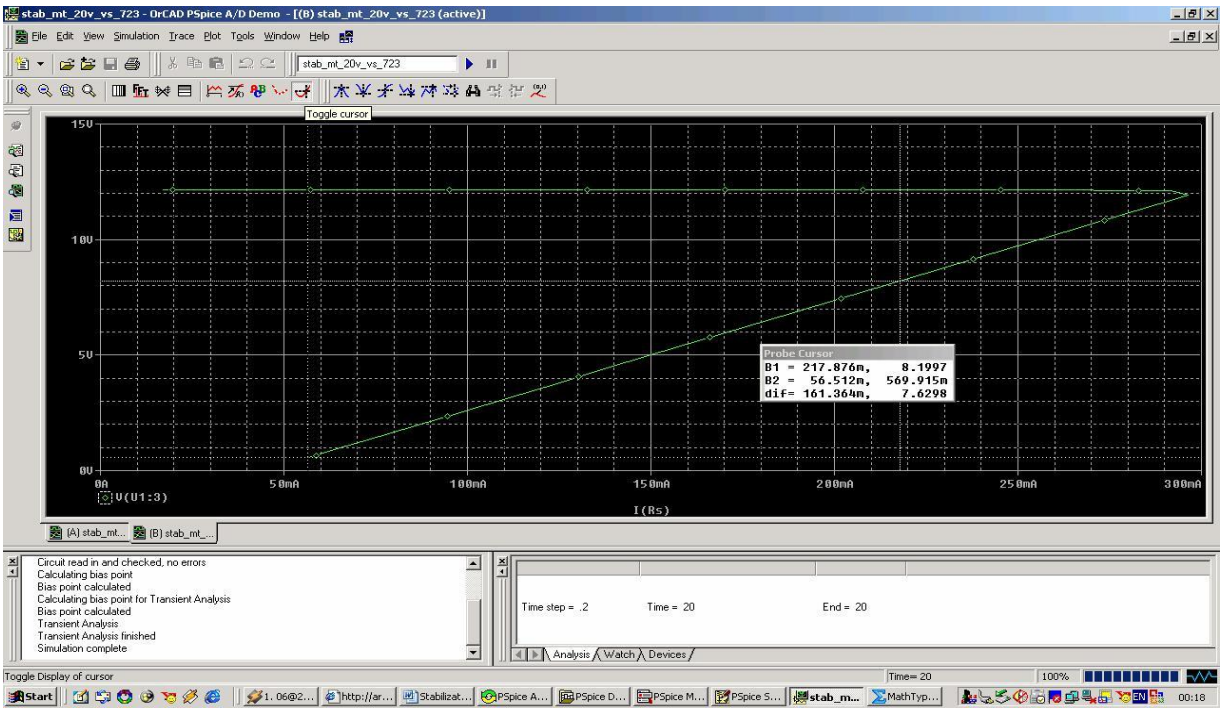


**Fig.17. The output characteristic $V_O$-$I_O$ of the voltage regulator for $V_O$>$V_R$ case**

It is required to measure:

A. The maximum output current value $I_{omax}$
B. The short circuit output current ( $I_O|_{R_S \to 0}$, in this case $R_S$ = 10Ω);
C. The value of the maximum power dissipation on the Q1 series pass transistor for $I_o$=$I_{omax}$ and $I_O|_{R_S \to 0}$ cases.

6. The output impedance $R_O = \frac{dV_O}{dI_O}$ and the line regulation $\frac{1}{S} = \frac{dV_O}{dV_i}$.

A. For the determination of the line regulation, a continuous DC voltage source (20 V) is mounted in series with a sinewave VS voltage (VSIN =1V). The load for the linear voltage regulator is a DC current source (IDC, 20mA). To obtain a real current source, an internal resistor ($R_i$ =10MΩ) is mounted in parallel with the current generator. The ambient temperature is kept constant (t=$27^0$C ). In table 3 are listed the voltage and the current sources used in the circuit (Fig.18). The simulation is performed in the time domain. The input and the output peak-to-peak voltages (V(Q1:c) , V(U1:3)) will be measured during a period. The line regulation (S) is the ratio between these voltages.

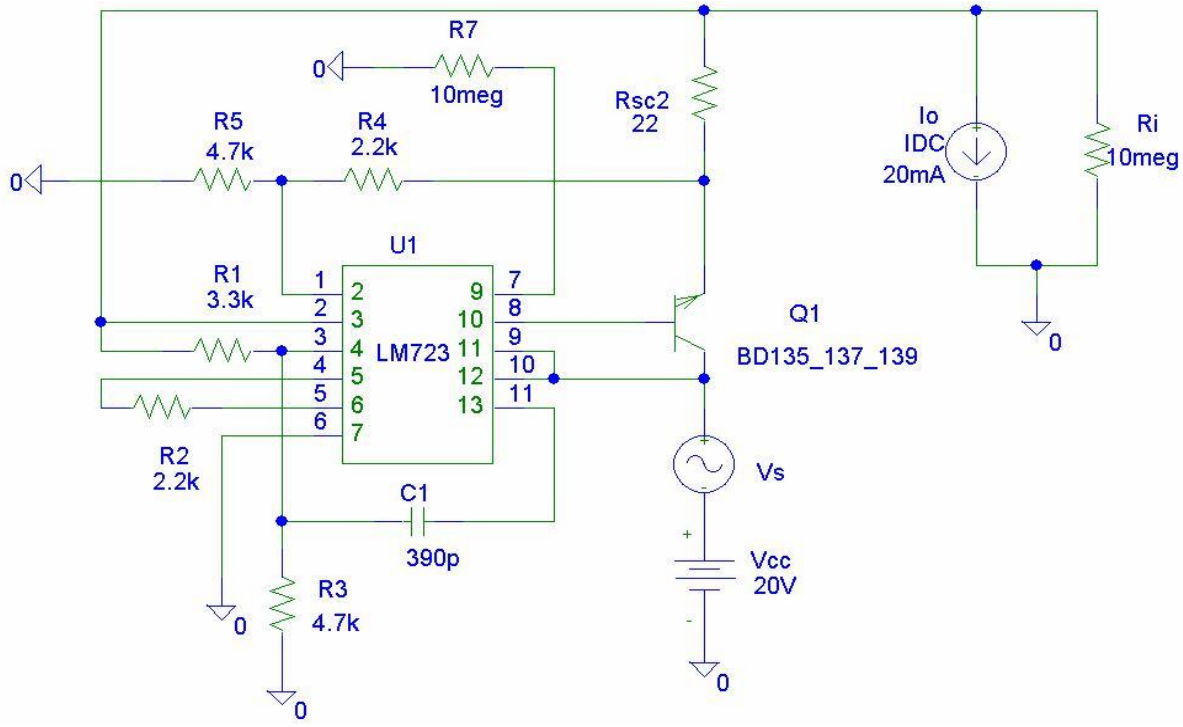


**Fig. 18. The circuit for the determination of the line regulation**

*Table 3*

| Name | Component | Value | Library |
|---|---|---|---|
| Vs | VSIN | VOFF=0, VAMPL=1, FREQ=50 | Source.slb |
| Io, Iodc | IDC | 20mA | Source.slb |
| Ioac | ISIN | IOFF=0, IAMPL=4mA, FREQ=50 | Source.slb |

B. For the determination of the output impedance ($R_O$), the circuit from Fig.19 is being drawn.

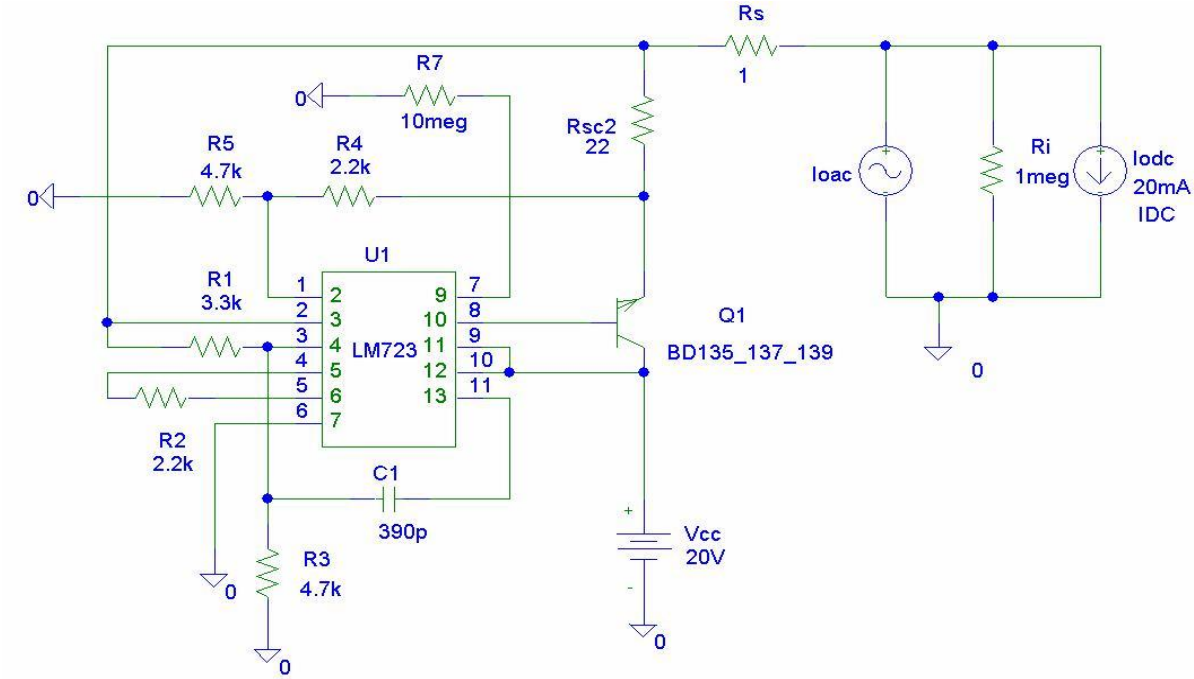


**Fig.19. The circuit for the determination of the output impedance ($R_O$)**

The Rs resistor is used to model the wires resistance, and the $R_i$ represents the internal impedance of the current sources. The output impedance ($R_O$) is the ratio between the output voltage (V(U1:3)) and the output current (I(Rs)).

*Annex 1*

**Instructions for installing Spice libraries to simulate the linear voltage regulator with LM723 (ßA723) integrated circuit.**

1. The files "stab.lib" and "stab.slb" should be copied in the folder where the Spice libraries are installed. For example, if the default setting are used, the path is: "C:\Program Files\ OrCAD_Demo\PSpice\Library"
2. In the Schematics editor will be added the paths to the libraries:

A. Analysis-Library and include files…-Browse…- C:\ Program Files\OrCAD_Demo\ PSpice\Library \stab.lib – Open- Add Library*-OK

B. Options-Editor Configuration-Library Settings…-Browse…- C:\ Program Files\OrCAD_Demo\ PSpice\Library \stab.slb- Open-Add*-OK-OK